TECHNICAL UNIVERSITY OF KOŠICE

FACULTY OF ELECTRICAL ENGINEERING AND INFORMATICS

DEPARTMENT OF ELECTRONICS AND MULTIMEDIA COMMUNICATIONS

BASIC OF ELECTRONICS

Lecture 9

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Applied Informatics

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We find the transconductance at the Q-point from the slope of the curve of Figure 4.8. This is given by

$$g_m = \frac{0.91 I_{DSS}}{0.64 V_p} = \frac{1.42\ I_{DSS}}{V_p} = -0.71 g_{mo}$$

These values usually represent a good starting point for setting the quiescent values for the JFET.

Example 4.1

Determine g_m for a JFET where $I_{DSS} = 7$ mA, $V_p = -3.5$ V, and $V_{DD} = 15$ V. Choose a reasonable location for the Q-point.

SOLUTION We start by referring to Figure 4.8 and selecting the Q-point as follows:

$$I_{DQ} = \frac{I_{DSS}}{2} = 3.5 \text{ mA}$$

$$V_{DSQ} = \frac{V_{DD}}{2} = 7.5 \text{ V}$$

$$V_{GSQ} = 0.3 V_p = -1.05 \text{ V}$$

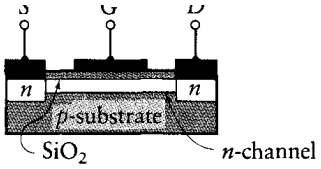
The transconductance, g_m, is found from the slope of the curve at the point $i_D/I_{DSS} = 0.5$ and $v_{GS}/V_p = 0.3$. Hence

$$g_m = \frac{1.42 I_{DSS}}{|V_p|} = \frac{1.42 \times 7 \text{ mA}}{3.5 \text{ V}} = 2840\ \mu\text{S}$$

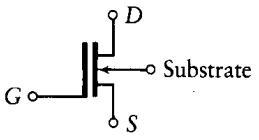
4.4 MOSFET Operation and Construction

In this section, we consider the metal-oxide-semiconductor FET (MOSFET). This FET is constructed with the gate terminal insulated from the channel with a silicon dioxide (SiO_2) dielectric and is constructed in either a *depletion* or an *enhancement* mode. We define and consider these two types in the next sections.

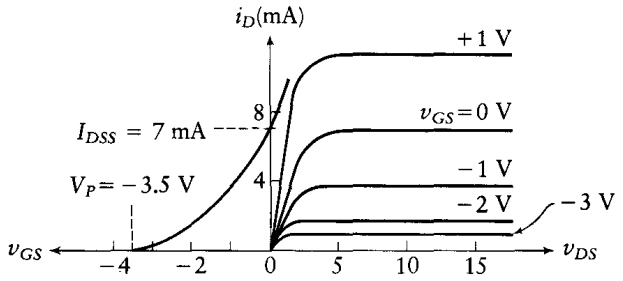
Figure 4.9
The n-channel depletion MOSFET.



(a) **Schematic of physical structure**



(b) **Symbol**



(c) **Transfer and i_D-v_{GS} characteristics**

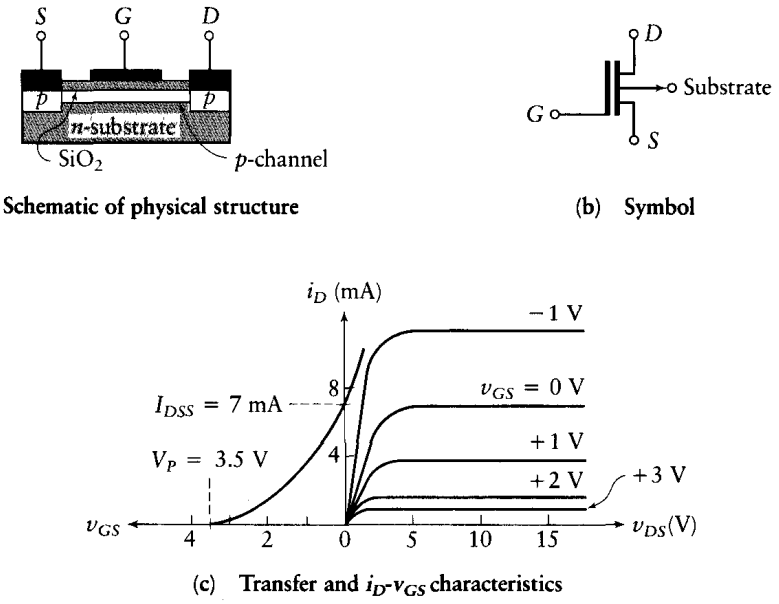
DCHUDOBNUENA

4.4.1 *Depletion MOSFET*

The constructions of the n-channel and the p-channel depletion MOSFET are shown in Figures 4.9 and 4.10, respectively. Each of these figures shows the construction, the symbol, the transfer characteristic, and the i_D-v_{GS} characteristics. The depletion MOSFET is constructed (as shown in Figure 4.9(a) for the n-channel and Figure 4.10(a) for the p-channel) with a physical channel constructed between the drain and the source. As a result, i_D exists between drain and source when a voltage, v_{DS}, is applied.

The n-channel depletion MOSFET of Figure 4.9 is established on a p-substrate, which is a p-doped silicon. The n-doped source and drain wells form low-resistance connections between the ends of the n-channel and the aluminimum contacts of the source (S) and the drain (D). An SiO_2 layer, which is an insulator, is grown on the top surface of the n-channel, as shown in Figure 4.9(a). An aluminum pad is deposited on the SiO_2 insulator to form the gate (G) terminal. The performance of the depletion MOSFET, as can be seen from Figures 4.9(c) and 4.10(c), is similar to that of the JFET. The JFET is controlled by the pn junction between the gate and the drain end of the channel. No such junction exists in the enhancement MOSFET, and the SiO_2 layer acts as the insulator. For the n-channel MOSFET, shown in Figure 4.9, a negative v_{GS} will push the electrons out of the channel region, hence depleting the channel. When v_{GS} reaches V_p, the channel will be pinched off. Positive values of v_{GS}

Figure 4.10
The *p*-channel depletion MOSFET.



(a) Schematic of physical structure (b) Symbol

(c) Transfer and i_D-v_{GS} characteristics

increase channel size, resulting in an increase of drain current. This is indicated on the characteristic curves of Figure 4.9(c).

Notice that the depletion MOSFET can operate with either positive or negative values of v_{GS}. We can use the same Shockley equation (equation (4.1)) to approximate the curves for negative v_{GS}. Notice, however, that the transfer characteristic continues on for positive values of v_{GS}. Since the gate is insulated from the channel, the gate current is negligibly small (10^{-12} A), and v_{GS} can be of either polarity.

As we can see from Figures 4.9(b) and 4.10(b), the symbol for the MOSFET has a fourth terminal, the *substrate*. The arrowhead points in for an *n*-channel and out for a *p*-channel. The *p*-channel depletion MOSFET, which is shown in Figure 4.10, is the same as Figure 4.9, except we reverse the *n*- and *p*-materials and reverse the polarity of the voltages and currents.

Example 4.2

Calculate the drain current, i_D, for the depletion MOSFET of Figure 4.9 with the following values of v_{GS}:

a. $v_{GS} = -1$V
b. $v_{GS} = -2$ V
c. $v_{GS} = -3$ V
d. $v_{GS} = +0.5$ V

SOLUTION We use equation (4.1) for each case, where $I_{DSS} = 7$ mA and $V_p = -3.5$ V.

$$\text{a. } i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2 = 7\left(1 - \frac{-1}{-3.5}\right)^2 = 3.57 \text{ mA}$$

$$\text{b. } i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2 = 7\left(1 - \frac{-2}{-3.5}\right)^2 = 1.29 \text{ mA}$$

$$\text{c. } i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2 = 7\left(1 - \frac{-3}{-3.5}\right)^2 = 0.14 \text{ mA}$$

$$\text{d. } i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2 = 7\left(1 - \frac{0.5}{-3.5}\right)^2 = 9.14 \text{ mA}$$

It is interesting to note that i_D increases dramatically as v_{GS} becomes positive. The accuracy of the formula approximation deteriorates for positive values of v_{GS}.

4.4.2 *Enhancement MOSFET*

The enhancement MOSFET is shown in Figure 4.11. It differs from the depletion MOSFET in that it does not have the thin n-layer but requires a positive voltage between the gate and source to establish a channel. This channel is formed by the action of a positive gate-to-source voltage, v_{GS}, which attracts electrons from the substrate region between the n-doped drain and source. Positive v_{GS} causes electrons to accumulate at the surface beneath the oxide layer. When the voltage reaches a threshold value, V_T, enough electrons are attracted to this region to make it act like a conducting n-channel. No appreciable current i_D will exist until v_{GS} exceeds V_T.

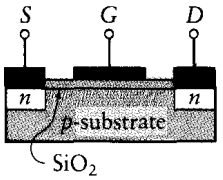
No value of I_{DSS} exists for the enhancement MOSFET, since the drain current is zero until the channel has been formed. I_{DSS} is zero at $v_{GS} = 0$. For values of

$$v_{GS} > V_T$$

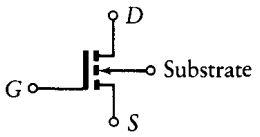
the drain current in saturation can be calculated from the equation

$$i_D = k(v_{GS} - V_T)^2 \tag{4.10}$$

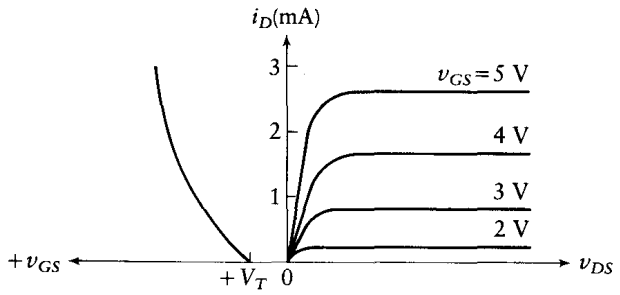
The value of k depends upon the construction of the MOSFET and is primarily a function of the width and length of the channel. A typical value for k is 0.3 mA/V^2, and the threshold voltage, V_T, is specified by the manufacturer. We



(a) Schematic of physical structure



(b) Symbol



(c) Transfer and i_D-v_{DS} characteristics

Figure 4.11
The n-channel enhancement MOSFET.

can find a value for g_m by differentiating equation (4.10), as we did with JFETs, with the result

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = 2k(v_{GS} - V_T) \tag{4.11}$$

If

$$v_{GS} < V_T$$

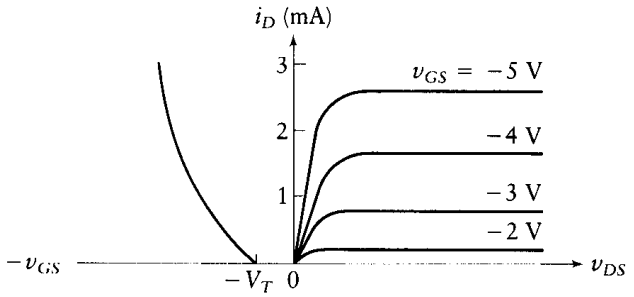
then $i_D = 0$.

The p-channel enhancement MOSFET is shown in Figure 4.12 and, as can be seen, displays similar but opposite characteristics to those of the n-channel enhancement MOSFET.

Although it is more restricted in operating range than the depletion MOSFET, the enhancement MOSFET is useful in IC applications (see Chapter 15) because of its small size and simple construction. The gate for both n- and p-channel MOSFETs is a metal deposit on a silicon-oxide layer. The construction begins with a substrate material (p-type for n-channel; n-type for p-channel) on which the opposite type of material is diffused to form the source and drain. Notice that the symbol for an enhancement MOSFET, which is shown in Figures 4.11 and 4.12, shows a broken line between source and drain to indicate that no channel initially exists.

Figure 4.12
The *p*-channel enhancement MOSFET.

(a) Schematic of physical structure (b) Symbol



(c) Transfer and i_D-v_{GS} characteristics

Example 4.3

Determine i_D for an *n*-channel enhancement MOSFET with $V_T = 3.0$ V when $k = 0.3$ mA/V^2 and v_{GS} is given by the following values:

a. 3.0 V
b. 4.0 V
c. 5.0 V

SOLUTION From equation (4.10) we calculate the following values.

a. $i_D = 0.3(v_{GS} - V_T)^2 = 0.3(3 - 3)^2 = 0$ mA
b. $i_D = 0.3(4 - 3)^2 = 0.3$ mA
c. $i_D = 0.3(5 - 3)^2 = 1.2$ mA

4.5 Biasing of FETs

The same basic circuits of Figure 3.6 that are used for biasing BJTs can also be used for JFETs and depletion MOSFETS. However, for the active region of the JFET and the depletion-mode MOSFET, the polarity of v_{GS} can be opposite from that of the drain voltage source. In selecting the operating point, voltage

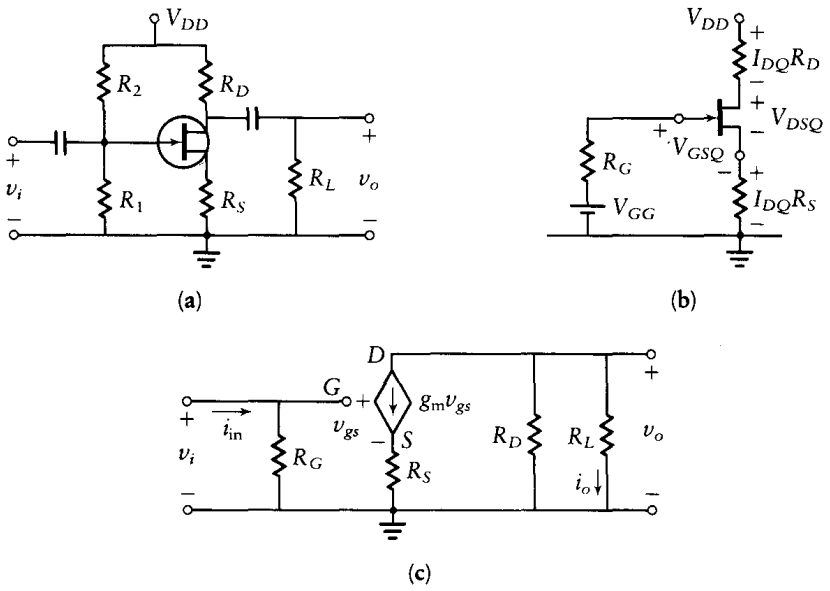


Figure 4.13
FET amplifier.

of the opposite polarity is not available from the source to meet the requirements of the circuit. It may be necessary to delete R_2 (see Figure 4.13) so only voltage of correct polarity is acquired. It is not always possible to find resistor values to achieve a particular Q-point. In such instances, selecting a new Q-point can sometimes provide a solution to the problem.

We consider here the bias equations for the CS amplifier, shown in Figure 4.13, where we use a JFET. The bias methods are similar for depletion MOSFETs.

Figure 4.13(a) illustrates a FET amplifier using one dc voltage source for biasing. We form the Thevenin equivalent of the bias circuit to obtain

$$R_G = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{4.12a}$$

$$V_{GG} = \frac{V_{DD} R_1}{R_1 + R_2} \tag{4.12b}$$

Since we have three unknown variables, I_{DQ}, V_{GSQ}, and V_{DSQ}, we need three dc equations. First, the dc equation around the gate-source loop is formed from Figure 4.13(b), as follows:

$$V_{GG} = V_{GSQ} + I_{DQ} R_S \tag{4.13}$$

Notice that since the gate current is zero, a zero voltage drop exists across R_G.

A second dc equation is found from the Kirchhoff's law equation in the drain-source loop, as follows:

$$V_{DD} = V_{DSQ} + I_{DQ}(R_S + R_D) \tag{4.14}$$

The third dc equation necessary to establish the bias point is found from equation (4.1), which is repeated here with $i_D = I_{DQ}$ and $v_{GS} = V_{GSQ}$.

$$\frac{I_{DQ}}{I_{DSS}} = \left(1 - \frac{V_{GSQ}}{V_p}\right)^2 \tag{4.15}$$

These three equations are sufficient to establish the bias for the JFET and depletion MOSFET, which are used for linear amplifiers. The enhancement MOSFET is used for digital ICs.

Note that we do not need to put the Q-point in the center of the ac load line as we did for BJT biasing. This is because we normally use a FET amplifier at the input to the amplifier to take advantage of the high input resistance. At this point, the voltage levels are so small that we do not drive the amplifier with large excursions. Also, since the FET characteristic curves are nonlinear, we would produce distortion with large input excursions.

4.6 Analysis of a CS Amplifier

Figure 4.13(c) shows the ac equivalent circuit for the FET amplifier. We assume r_{DS} is large compared to $R_D \| R_L$, so it can be neglected. Writing a KVL equation around the gate circuit, we find

$$v_{gs} = v_i - R_S i_D = v_i - R_S g_m v_{gs}$$

Solving for v_{gs} yields

$$v_{gs} = \frac{v_i}{1 + R_S g_m}$$

The output voltage, v_o, is given by

$$v_o = -i_d(R_D \parallel R_L) = \frac{-(R_D \parallel R_L) g_m v_i}{1 + R_S g_m}$$

The voltage gain, A_v, is

$$A_v = \frac{v_o}{v_i} = \frac{-g_m(R_D \parallel R_L)}{1 + R_S g_m}$$

$$= \frac{-(R_D \parallel R_L)}{R_S + 1/g_m} \tag{4.16a}$$

The resistance, R_S, is sometimes bypassed by a capacitor, in which case the voltage gain increases to

$$A_v = -g_m(R_D \parallel R_L)$$

The input resistance and current gain are given by

$$R_{\text{in}} = R_G = R_1 \parallel R_2 \tag{4.16b}$$

$$A_i = \frac{i_o}{i_{\text{in}}} = \frac{A_v R_{\text{in}}}{R_L} = \frac{-R_D \parallel R_L}{R_S + 1/g_m} \frac{R_{\text{in}}}{R_L} = \frac{-R_G}{R_S + 1/g_m} \frac{R_D}{R_D + R_L} \tag{4.16c}$$

Example 4.4 CS Amplifier (Analysis)

Find A_v for the JFET amplifier of Figure 4.14(a). The Q-point is at V_{DSQ} = 12 V and I_{DQ} = 7 mA. The FET parameters are given by

g_m = 3.0 mS

r_{DS} = 200 kΩ

SOLUTION From the equivalent circuit of Figure 4.14(b), we obtain

$$A_v = \frac{v_o}{v_{gs}} = \frac{-i_D(R_D \parallel r_{DS})}{v_{gs}} = -g_m(R_D \parallel r_{DS}) = 52$$

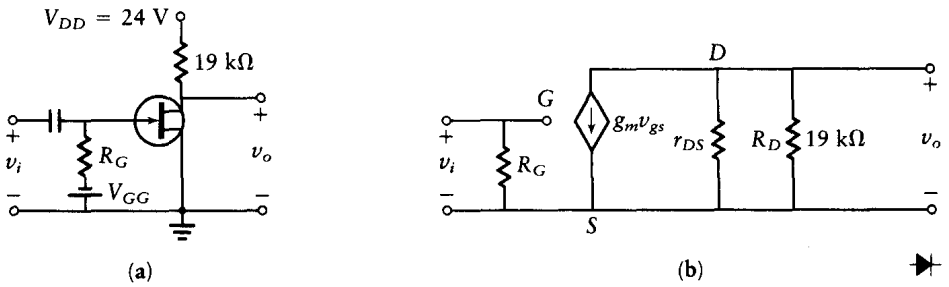


Figure 4.14
JFET circuit for Example 4.4.

4.7 Design of a CS Amplifier

The design procedure of a CS amplifier is presented in this section. The JFET and the depletion MOSFET amplifier design is presented as a step-by-step procedure. You should convince yourself that you understand the origin of each step, since several variations may subsequently be required.

Amplifiers are designed to meet gain requirements if the desired specifications are within the range of the transistor. The supply voltage, load resistance, voltage gain and input resistance (or current gain) are usually specified. Our problem is to select the resistance values R_1, R_2, R_D, and R_S. Refer to Figure 4.15 as you follow the steps in the procedure. This procedure assumes that a device has been selected and that its characteristics are known—at least V_p and I_{DSS}.

Step 1 Select a Q-point in the most linear portion of the JFET characteristic curves. Refer to the curves of Figure 4.15(b) for an example. This identifies V_{DSQ}, V_{GSQ}, I_{DQ}, and g_m. If an i_D-v_{GS} characteristic curve is unavailable, use the dimensionless curve of Figure 4.8, with I_{DSS} and V_p given for the transistor type used.

Step 2 Write the dc KVL equation (equation (4.14)) around the drain-source loop,

$$V_{DD} = V_{DSQ} + (R_S + R_D)I_{DQ}$$

Solving for the sum of the two resistors yields

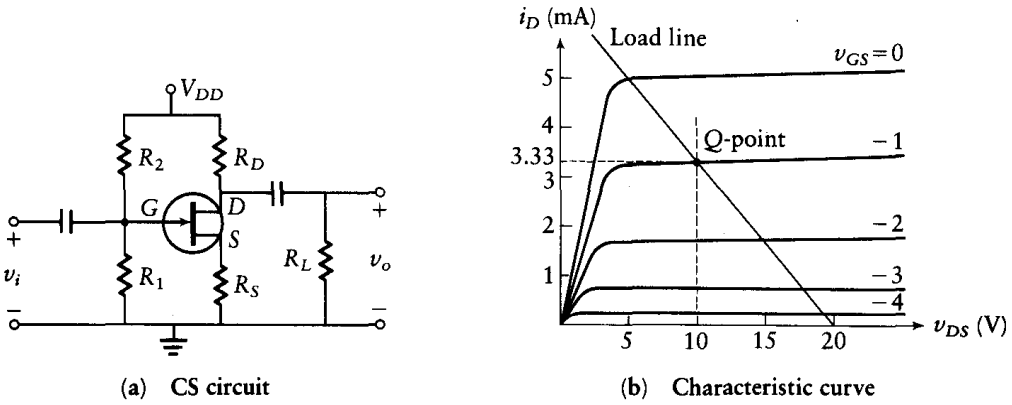
$$R_S + R_D = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} = K_1 \tag{4.17}$$

Equation (4.17) represents one equation in two unknowns, R_S and R_D.

Step 3 Use the voltage-gain equations (equation (4.16a)) to yield a second equation in R_S and R_D. We can substitute equation (4.17) into equation (4.16a)

$$A_v = \frac{-R_L \parallel R_D}{R_S + 1/g_m} = \frac{-R_L \parallel R_D}{(K_1 - R_D) + 1/g_m} \tag{4.18}$$

The resistance, R_D, *is the only unknown in this equation.* Solving for R_D results in a quadratic equation with two solutions, one negative and one positive. If the positive solution results in $R_D > K_1$, thus implying a negative R_S, a new



(a) CS circuit (b) Characteristic curve

Figure 4.15
JFET CS amplifier.

Q-point must be selected (i.e., restart the design at Step 1). If the positive solution yields $R_D < K_1$, we can proceed to Step 4.

Step 4 Solve for R_S using equation (4.17), the drain-to-source loop equation developed in Step 2.

$$R_S = \frac{V_{DD} - V_{DSQ}}{I_{DQ}} - R_D$$

With R_D and R_S known, we need find only R_1 and R_2.

Step 5 Write the KVL equation for the gate-source loop (equation (4.13)):

$$V_{GG} = V_{GSQ} + I_{DQ}R_S$$

The voltage V_{GSQ} is of opposite polarity from V_{DD}. Thus the term $I_{DQ}R_S$ must be greater than V_{GSQ} in magnitude. Otherwise, V_{GG} will have the opposite polarity from V_{DD}, which is not possible according to equation (4.12b).

Step 6 We now solve for R_1 and R_2 assuming that the V_{GG} found in Step 5 has the *same polarity* as V_{DD}. These resistor values are selected by finding the value of R_G from the current-gain equation or from the input resistance. We solve equation (4.12) to find R_1 and R_2:

$$R_1 = \frac{R_G}{1 - V_{GG}/V_{DD}}$$

$$R_2 = \frac{R_G V_{DD}}{V_{GG}}$$

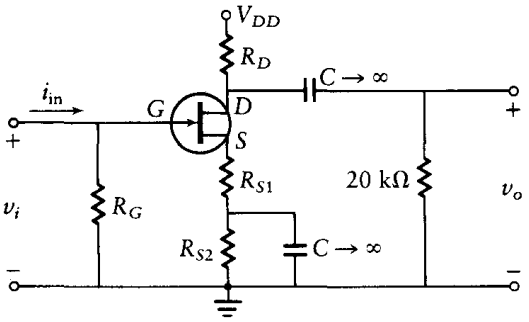


Figure 4.16
JFET design with bypassed source resistor.

Step 7 If V_{GG} has the *opposite polarity* of V_{DD}, it is not possible to solve for R_1 and R_2. The practical way to proceed is to let $V_{GG} = 0$ V. Thus, $R_2 \to \infty$. Since V_{GG} is specified by equation (4.13), the previously calculated value of R_S now needs to be modified. In Figure 4.16, where a capacitor is used to bypass a part of R_S, we develop the new value of R_S as follows:

$$V_{GG} = 0 = V_{GSQ} + I_{DQ}R_{Sdc}$$

Therefore, solving for R_{Sdc} yields

$$R_{Sdc} = \frac{-V_{GSQ}}{I_{DQ}}$$

The value of R_{Sdc} is $R_{S1} + R_{S2}$ and the value of R_{Sac} is R_{S1}.

Now that we have a new R_{Sdc}, we must repeat several steps.

Step 8 Determine R_D using KVL for the drain-to-source loop (repeat Step 2):

$$R_D = K_1 - R_{Sdc}$$

The design problem now becomes one of calculating both R_{S1} and R_{S2} instead of finding only one source resistor.

With a new value for R_D of $K_1 - R_{Sdc}$, we go to the voltage-gain expression of equation (4.16a) with R_{Sac} used for this ac equation rather than R_S.

The following additional steps must be added to the design procedure.

Step 9 We find R_{Sac} (which is simply R_{S1}) from the voltage-gain equation, equation (4.16a):

$$A_v = \frac{-(R_L \| R_D)}{R_{Sac} + 1/g_m}$$

R_{Sac} is the only unknown in this equation. Therefore,

$$R_{Sac} = -\frac{R_L \| R_D}{A_v} - \frac{1}{g_m}$$

Suppose now that R_{Sac} is found to be positive but less than R_{Sdc}. This is the desirable condition since

$$R_{Sdc} = R_{Sac} + R_{S2}$$

Then our design is complete and

$$R_1 = R_{\text{in}} = R_G$$

Step 10 Suppose that R_{Sac} is found to be positive but *greater* than R_{Sdc}. The amplifier cannot be designed with the voltage gain and Q-point as selected. A new Q-point must be selected, and we return to Step 1. If the voltage gain is too high, it may not be possible to effect the design with any Q-point. A different transistor may be needed or the use of two separate stages may be required.

4.8 Selection of Components

A design is not yet complete when the various component values are specified. It is still necessary to select the actual components to be used (e.g., choose the manufacturer's part numbers from a catalog). Thus, when the design requires a resistor value, say 102.5 Ω, the designer will not be able to find this resistor in a standard parts catalog. Available nominal component values depend upon tolerances. As an example, a 100-Ω resistor with a 5% tolerance can have any value between 95 Ω and 105 Ω. It would not make much sense for the manufacturer to offer another off-the-shelf resistor with a nominal rating of 101 Ω, since that resistor could have a value between approximately 96 Ω and 106 Ω. The distance between adjacent nominal component values is therefore related to the tolerance, with such distance decreasing as the tolerance decreases (i.e., higher-precision components). Standard values of resistors and capacitors are included in Appendix E.

Since component values are not readily available to any degree of resolution, it would not make sense to carry out design calculations to an unreasonably large number of significant figures.

In our design examples, we specify values to at least three significant figures. This is important to ensure that we still maintain accuracy to two significant