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BASIC OF ELECTRONICS

Lecture 8

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Applied Informatics

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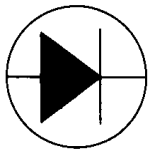

FIELD-EFFECT TRANSISTOR AMPLIFIERS

4.0 Introduction

The performance of the *field-effect transistor (FET),* which was proposed by W. Shockley in 1952, is different from that of the BJT. The controlling parameter for an FET is *voltage* instead of *current.*

The FET is a *unipolar* device, since current exists *either* as electrons or holes. In an *n*-channel FET, electron current exists, and in a *p*-channel FET, hole current exists. Both types of FET are controlled by a voltage imposed between the *gate* and the *source.*

In comparing FETs to BJTs, we notice that the *drain* (*D*) is analogous to the collector and the *source* (*S*) is analogous to the emitter. A third contact, the *gate* (*G*), is analogous to the base. The source and drain of an FET can usually be interchanged without affecting transistor operation.

This chapter begins with a discussion of the FET characteristics and a comparison of these characteristics with the characteristics of the BJT. The construction and operation of both JFETs and MOSFETs are then described. We develop the biasing techniques for FETs followed by ac analysis using equivalent circuits. We then derive the gain equations for the common-source (CS) amplifier. This is followed by development of a step-by-step design procedure, which is applied to several design examples.

Analysis and design of common-drain (CD) (source follower (SF)) amplifiers are then presented. Step-by-step design procedures are developed followed by application of these procedures to examples.

The chapter concludes with a brief discussion of other speciality devices.

4.1 Advantages and Disadvantages of the FET

The advantages of FETs can be summarized as follows:

1. They are voltage-sensitive devices with high input impedance (on the order of 10^7 to 10^{12} Ω). Since this input impedance is considerably higher than that of BJTs, FETs are preferred over BJTs for use as the input stage to a multistage amplifier.
2. FETs generate a lower noise level than BJTs.
3. FETs are more temperature stable than BJTs.
4. FETs are generally easier to fabricate than BJTs, since they usually require fewer masking steps and fewer diffusions. Greater numbers of devices can be fabricated on a single chip (i.e., increased *packing density* is possible).
5. FETs react like voltage-controlled variable resistors for small values of drain source voltage.
6. The high input impedance of FETs permit them to store charge long enough to allow use as storage elements.
7. Power FETs can dissipate high power and can switch large currents.

There are several disadvantages that limit the use of FETs in some applications:

1. FETs usually exhibit poor frequency response because of high input capacitance.
2. Some types of FETs exhibit poor linearity.
3. FETs can be damaged in handling due to static electricity.

4.2 Types of FETs

We consider here three major types of FETs:

1. Junction FET (JFET)
2. Depletion-mode metal-oxide semiconductor FET (depletion MOSFET)

3. Enhancement-mode metal-oxide semiconductor FET (enchancement MOSFET)

The MOSFET is often called an insulated-gate FET (IGFET).

4.3 JFET Operation and Construction

Like the BJT, the FET is a three-terminal device, but it has only one *pn* juncton rather than two, as in the BJT. A schematic for the physical structure of the JFET is shown in Figure 4.1.

The *n*-channel JFET, shown in Figure 4.1(a), is constructed using a strip of *n*-type material with two *p*-type materials diffused into the strip, one on each side. The *p*-channel JFET has a strip of *p*-type material with two *n*-type materials diffused into the strip, as shown in Figure 4.1(b).

To understand the operation of the JFET, we connect the *n*-channel JFET of Figure 4.1(a) to an external circuit. A supply voltage, V_{DD}, is applied to the drain (this is analogous to the V_{CC} supply voltage for a BJT) and the source is brought to common. A gate supply voltage, V_{GG}, is applied to the gate (this is analogous to V_{BB} for the BJT). This circuit configuration is shown in Figure 4.2(a).

V_{DD} provides a drain-source voltage, v_{DS}, that causes a drain current, i_D, from drain to source. The drain current, i_D, which is identical to the source current, exists in the channel surrounded by the *p*-type gate. The gate-to-source voltage, v_{GS}, which is equal to $-V_{GG}$ (see Figure 4.2(a)), creates a *depletion region* in the channel, which reduces the channel width and hence increases the resistance between drain and source. Since the gate-source junction is reverse-biased, a zero gate current results.

We consider JFET operation with $v_{GS} = 0$, as shown in Figure 4.2(b). The drain current, i_D, through the *n*-channel from drain to source causes a voltage drop along the channel, with the higher potential at the drain-gate junction. This positive voltage at the drain-gate junction reverse-biases the *pn* junction and produces a depletion region, as shown by the shaded area in Figure 4.2(b).

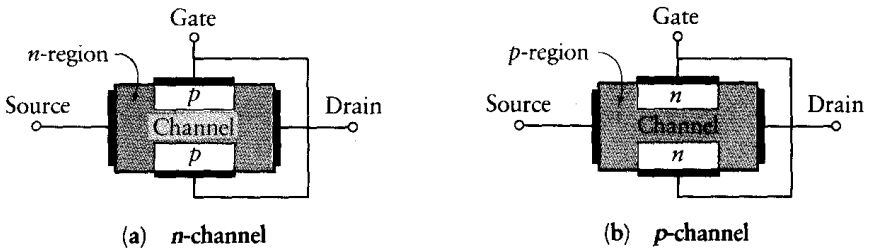

Figure 4.1
Physical structure of JFET.

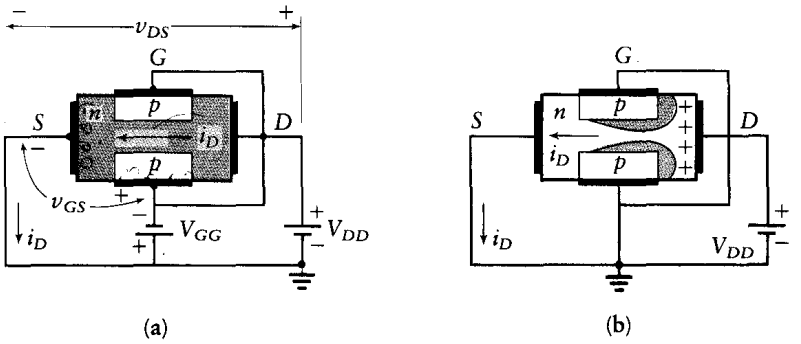

Figure 4.2
Operation of the JFET in an external circuit.

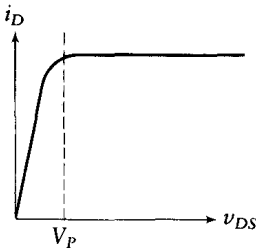

Figure 4.3
i_D-v_{DS} characteristic for n-channel JFET.

When we increase v_{DS}, the drain current, i_D, also increases, as shown in Figure 4.3. This action results in a larger depletion region and an increased channel resistance between drain and source. As v_{DS} is further increased, a point is reached where the depletion region forms across the entire channel and the drain current reaches its saturation point. If we increase v_{DS} beyond this point, i_D remains constant. The value of the saturated drain current with $V_{GS} = 0$ is an important parameter and is denoted as the *drain-source saturation current*, I_{DSS}. As can be seen from Figure 4.3, increasing v_{DS} beyond this channel *pinch-off* point causes no further increase in i_D, and the i_D-v_{DS} characteristic curve becomes flat (i.e., i_D remains constant as v_{DS} is further increased).

4.3.1 *JFET Gate-to-Source Voltage Variation*

In the previous section, we developed the i_D-v_{DS} characteristic curve with $v_{GS} = 0$. In this section, we consider the complete i_D-v_{DS} characteristics for various values of the v_{GS} parameter. Note that in the case of the BJT, the characteristic curves (i_C-v_{CE}) have i_B as the parameter. The FET is a voltage-controlled device and is controlled by v_{GS}. Figure 4.4 shows the i_D-v_{DS} characteristic curves for both the n-channel and p-channel JFET. Before we discuss these curves, take note of the symbols for an n-channel and a p-channel JFET, which are also shown in Figure 4.4. These symbols are the same except for the direction of the arrow.

As v_{GS} is increased (more negative for an n-channel and more positive for a p-channel) the depletion region is formed and closes off for a lower value of i_D. Hence, for the n-channel JFET of Figure 4.4(a), the maximum i_D reduces from I_{DSS} as v_{GS} is made more negative. If v_{GS} is further decreased (more negative), a value of v_{GS} is reached, after which i_D will be zero regardless of the value of v_{DS}. This value of v_{GS} is called V_{GSOFF}, or *pinch-off voltage* (V_p). The value of V_p is negative for an n-channel JFET and positive for a p-channel JFET.

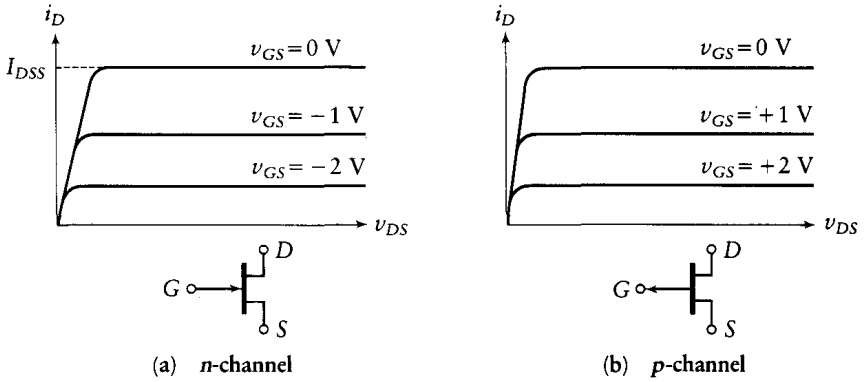

Figure 4.4
i_D-v_{DS} characteristic curves for JFET.

4.3.2 *JFET Transfer Characteristics*

Of great value in JFET design is the transfer characteristic, which is a plot of the drain current, i_D, as a function of gate-to-source voltage, v_{GS}, above pinch-off. Although this is plotted with v_{DS} equal to a constant, the transfer characteristic is essentially independent of v_{DS} since, after the FET reaches pinch-off, i_D remains constant for increasing values of v_{DS}. This can be seen from the i_D-v_{DS} curves of Figure 4.4, where each curve becomes flat for values of $v_{DS} > V_p$. Each curve has a different saturation point.

In Figure 4.5, we show the transfer characteristics and the i_D-v_{GS} characteristics for an n-channel JFET. We plot these with a common i_D axis. The transfer characteristics can be obtained from an extension of the i_D-v_{DS} curves. A useful method of determining the transfer characteristic is with the following relationship (the Shockley equation):

$$\frac{i_D}{I_{DSS}} \approx \left(1 - \frac{v_{GS}}{V_p}\right)^2 \tag{4.1}$$

Hence, we need to know only I_{DSS} and V_p, and the entire characteristic is then determined. Manufacturer's data sheets often give these two parameters, so the transfer characteristic can be constructed or equation (4.1) can be used directly. Note that i_D saturates (i.e., becomes constant) as v_{DS} exceeds the voltage necessary for the channel to pinch off. This can be expressed as an equation for $v_{DS(sat)}$ for each curve, as follows:

$$v_{DS(sat)} = v_{GS} + V_p$$

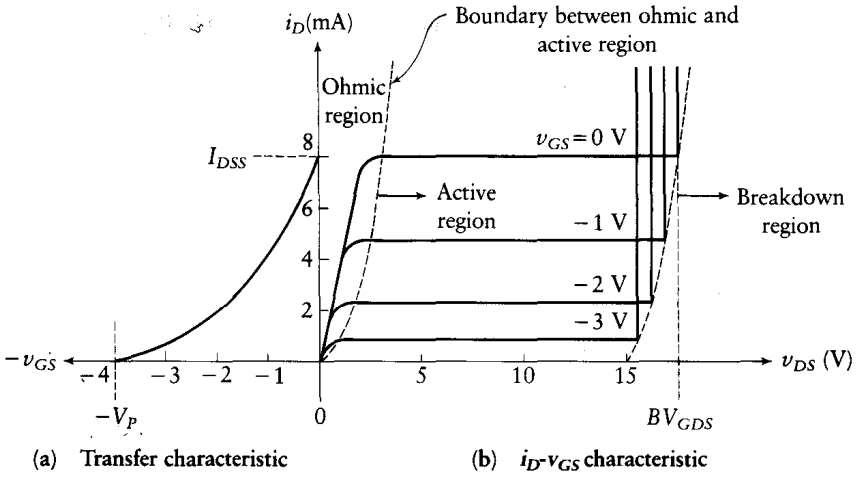

Figure 4.5
JFET characteristics.

As v_{GS} becomes more negative, the pinch-off occurs at lower values of v_{DS} and the saturation current becomes smaller. The useful region for linear operation is above pinch-off and below the breakdown voltage. In this region, i_D is saturated and its value depends upon v_{GS}, according to equation (4.1) or the transfer characteristic.

The transfer and i_D-v_{GS} characteristic curves for the JFET, which are shown in Figure 4.5, are different from the similar curves for a BJT: The FET is a voltage-controlled device, whereas the BJT is a current-controlled device. The controlling parameter for the FET is gate-source voltage rather than base current, as in the BJT.

There are two other distinct differences between the FET and BJT. First, the vertical spacing between pairs of parametric curves for the FET is not linearly related to the value of the controlling parameter. Thus, for example, the distance between the $v_{GS} = 0$ V curve and $v_{GS} = -1$ V curve in Figure 4.5 is not the same as that between the $v_{GS} = -1$ V curve and $v_{GS} = -2$ V curve. This contrasts with the BJT curves, where a more linear relationship exists.

The second difference relates to the size and shape of the ohmic region of the characteristic curves. Recall that in using BJTs, we avoid nonlinear operation by not using the transistor at the lower 5% of values of v_{CE}, which is called the *saturation region*. We see that the width of the ohmic region for the JFET is a function of the gate-to-source voltage. As the magnitude of the gate-to-source voltage decreases, the width of the ohmic region increases. We also note from Figure 4.5 that the breakdown voltage is a function of the gate-to-source voltage. In fact, to obtain reasonably linear signal amplification, we

must utilize only a relatively small segment of these curves—the area of linear operation is in the active region.

Note from Figure 4.5 that as v_{DS} increases from zero, a break point occurs on each curve, beyond which the drain current increases very little as v_{DS} continues to increase. At this drain-to-source voltage, pinch-off occurs. The pinch-off values in Figure 4.5 are connected with a dashed curve that separates the ohmic region from the active region. As v_{DS} continues to increase beyond the pinch-off point, a point is reached where the voltage between drain and source becomes so large that *avalanche breakdown* occurs. (This phenomenon also occurs in diodes and in BJTs.) At the breakdown point, i_D increases sharply with a negligible increase in v_{DS}. This breakdown occurs at the drain end of the gate-channel junction. Hence, when the drain-gate voltage, v_{DG}, exceeds the breakdown voltage, BV_{GDS} (for $v_{GS} = 0$ V), for the *pn* junction, avalanche occurs. At this point, the i_D-v_{DS} characteristic exhibits the peculiar shape shown on the right part of Figure 4.5.

The region between pinch-off and avalanche breakdown is called the *active region, amplifier operating region, saturation region,* or *pinch-off region,* as shown in Figure 4.5. The ohmic region (before pinch-off) is sometimes called the *voltage-controlled region.* The FET is operated in this region both when a variable resistor is desired and in switching applications.

The breakdown voltage is a function of v_{GS} as well as v_{DS}. As the magnitude of the voltage between gate and source is increased (more negative for *n*-channel and more positive for *p*-channel), the breakdown voltage decreases. With $v_{GS} = V_p$, the drain current is zero (except for a small leakage current), and with $v_{GS} = 0$, the drain current saturates at a value

$$i_D = I_{DSS}$$

where I_{DSS} is the *saturation drain-to-source current.*

Between pinch-off and breakdown, the drain current is saturated and does not change appreciably as a function of v_{DS}. After the FET passes the pinch-off operating point, the value of i_D can be obtained from the characteristic curves or from equation (4.1), which is repeated here for reference.

$$i_D \approx I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2$$

The saturation drain-to-source current, I_{DSS}, is a function of temperature,

$$I_{DSS} = KT^{-3/2}$$

where K is a constant [51]. The pinch-off voltage is an approximately linear

function of temperature (as is the case with the base-emitter current in the BJT); hence

$$\Delta V_p = -k_p \Delta T$$

where $k_p \approx 2$ mV/°C.

The currents and voltages in this section are presented for an n-channel JFET. The values for a p-channel JFET are the reverse of those just given for the n-channel.

4.3.3 *Equivalent Circuit, g_m and r_{DS}*

In order to obtain a measure of the amplification possible with a JFET, we introduce the parameter g_m, which is the *forward transconductance*. This parameter is similar to the current gain (or h_{fe}) for a BJT. The value of g_m, which is measured in siemens (S), is a measure of the change in drain current for a change in gate-source voltage. This can be expressed as

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \approx \frac{\Delta i_D}{\Delta v_{GS}} \bigg|_{V_{DS}=\text{constant}} \tag{4.2}$$

The transconductance, g_m, does not remain constant as the Q-point is changed. This can be seen by geometrically determining g_m from the transfer characteristic curves. As i_D changes, the slope of the transfer characteristic curve of Figure 4.5 varies, thereby changing g_m.

We can find the transconductance by differentiating equation (4.1), with the result

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{2I_{DSS}(1 - v_{GS}/V_p)}{-V_p} \tag{4.3}$$

We define

$$g_{mo} = \frac{2I_{DSS}}{-V_p}$$

which is the transconductance at $v_{GS} = 0$. Using this equation, the transconductance is given by

$$g_m = g_{mo}\left(1 - \frac{v_{GS}}{V_p}\right) \tag{4.4}$$

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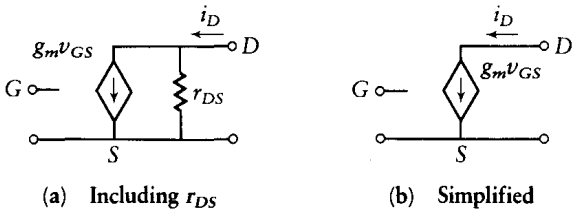

Figure 4.6
FET equivalent circuit.

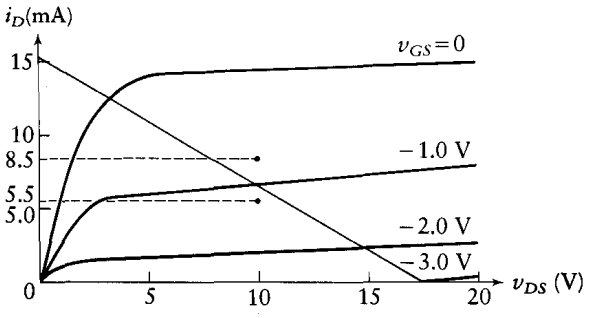

Figure 4.7
i_D-v_{DS} JFET characteristic curves.

which leads to the equivalent circuit shown in Figure 4.6(a). Because r_{DS} is so large, we can usually use the simplified equivalent circuit of Figure 4.6(b) to determine the active region performance of a JFET. Equation (4.9) then reduces to

$$\Delta i_D = g_m \Delta v_{GS}$$

The performance of a JFET is specified by the values of g_m and r_{DS}. We now determine these parameters for an n-channel JFET using the characteristic curve shown in Figure 4.7. We select an operating region that is approximately in the middle of the curves, that is, between $v_{GS} = -0.8$ V and $v_{GS} = -1.2$ V and $i_D = 8.5$ mA and $i_D = 5.5$ mA. From equation (4.2), we find

$$g_m = \left.\frac{\Delta i_D}{\Delta v_{GS}}\right|_{v_{DS}=\text{constant}} = \frac{(5.5 - 8.5)\text{ mA}}{-1.2 - (-0.8)} = 7.5\text{ mS}$$

If the characteristic curves for a JFET are not available, g_m and v_{GS} can be obtained mathematically, provided I_{DSS} and V_p are known. These two parameters are usually given in the manufacturer's specifications. The quiescent drain current, I_{DQ}, can be selected to be between 0.3 and 0.7 times I_{DSS}, which locates the Q-point in the most linear region of the characteristic curves. Repeating equation (4.1), we have

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_p}\right)^2$$

and at the quiescent point,

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_p}\right)$$

where

$$g_{mo} = \frac{-2I_{DSS}}{V_p}$$

The relationship between i_D and v_{GS} can be plotted on a dimensionless graph (i.e., a normalized curve), as shown in Figure 4.8. The vertical axis of this graph is $i_D/|I_{DSS}|$, and the horizontal axis is $v_{GS}/|V_p|$. The slope of the curve is g_m.

A reasonable procedure for locating the quiescent value near the center of the linear operating region is as follows:

1. Select $I_{DQ} = I_{DSS}/2$ and, from the curve, $V_{GSQ} = 0.3V_p$. Note from Figure 4.8 that this is near the midpoint of the curve.
2. Select $V_{DSQ} = V_{DD}/2$.

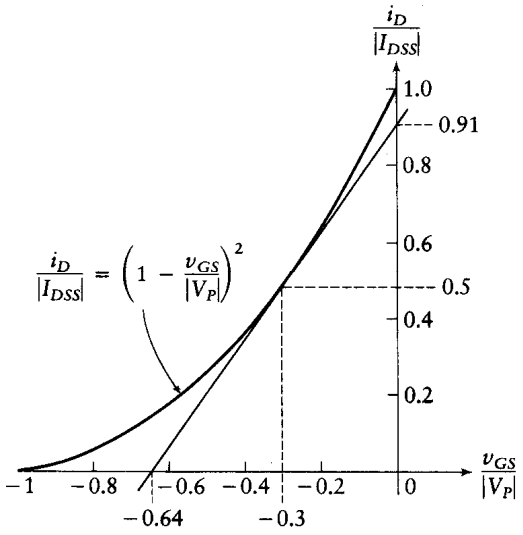

Figure 4.8 $i_D/|I_{DSS}|$ versus $v_{GS}/|V_p|$.

We find the transconductance at the Q-point from the slope of the curve of Figure 4.8. This is given by

$$g_m = \frac{0.91 I_{DSS}}{0.64 V_p} = \frac{1.42\ I_{DSS}}{V_p} = -0.71 g_{mo}$$

These values usually represent a good starting point for setting the quiescent values for the JFET.

Example 4.1

Determine g_m for a JFET where $I_{DSS} = 7$ mA, $V_p = -3.5$ V, and $V_{DD} = 15$ V. Choose a reasonable location for the Q-point.

SOLUTION We start by referring to Figure 4.8 and selecting the Q-point as follows:

$$I_{DQ} = \frac{I_{DSS}}{2} = 3.5 \text{ mA}$$

$$V_{DSQ} = \frac{V_{DD}}{2} = 7.5 \text{ V}$$

$$V_{GSQ} = 0.3 V_p = -1.05 \text{ V}$$

The transconductance, g_m, is found from the slope of the curve at the point $i_D/I_{DSS} = 0.5$ and $v_{GS}/V_p = 0.3$. Hence

$$g_m = \frac{1.42 I_{DSS}}{|V_p|} = \frac{1.42 \times 7 \text{ mA}}{3.5 \text{ V}} = 2840\ \mu\text{S}$$

4.4 MOSFET Operation and Construction

In this section, we consider the metal-oxide-semiconductor FET (MOSFET). This FET is constructed with the gate terminal insulated from the channel with a silicon dioxide (SiO_2) dielectric and is constructed in either a *depletion* or an *enhancement* mode. We define and consider these two types in the next sections.