TECHNICAL UNIVERSITY OF KOŠICE

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Lecture 5

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Applied Informatics

Contents

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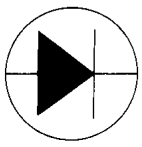


DESIGN OF BIPOLAR JUNCTION TRANSISTOR AMPLIFIERS

3.0 Introduction

In Chapter 2 we discuss the biasing, or dc operation, of BJT circuits. The transistor is biased to obtain the required peak-to-peak output voltage swing. In the current chapter we concentrate upon *small-signal analysis* through the use of equivalent circuit techniques. We describe the use of the equivalent circuit method using *hybrid parameters*. The transistor parameters required to accomplish this analysis can be obtained from manufacturer's data sheets. The data are provided by the manufacturers in a format as shown in the examples of Appendix D. The design method presented here reduces the dependence of the circuit upon the variations in the transistor parameters.

The chapter begins with an introduction to hybrid parameters that are used to develop a transistor mathematical model. We derive the equations for input resistance, voltage gain, current gain, and output resistance for the various amplifier configurations (i.e., CE, CC, and CB). In each case, both a precise and an approximate relationship are developed. Design examples are presented for each case. Multistage amplifier analysis is also discussed and example problems are given.

3.1 Analysis of Two-Port Networks

3.1.1 *Gain Impedance Formula*

We derive an important relationship between the ac quantities of voltage gain, A_v, and current gain, A_i. Figure 3.1 shows a block diagram of a four-terminal (two-port) network with input resistance R_{in} and load resistance, R_L, which are assumed to be resistors. In general, they can be complex impedances.

The relationships between the input variables, v_i and i_{in}, and the output variables, v_o and i_o, are derived directly from Ohm's law. That is,

$$v_o = i_o R_L$$

$$v_i = i_{in} R_{in}$$

Forming the ratio of these two equations yields

$$\frac{v_o}{v_i} = \frac{i_o}{i_{in}} \frac{R_L}{R_{in}}$$

Voltage gain is defined as

$$A_v = \frac{v_o}{v_i}$$

and current gain is defined as

$$A_i = \frac{i_o}{i_{in}}$$

Combining the various equations, we find

$$A_v = \frac{A_i R_L}{R_{in}} \tag{3.1}$$

Equation (3.1) is called the *gain impedance formula* and is used throughout this text.

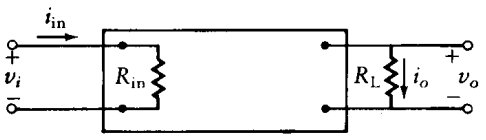


Figure 3.1
Two-port network.

3.1.2 *Hybrid Parameters*

There are a number of ways to characterize four-terminal networks. In a four-terminal system, there are four circuit variables: the input voltage and current and the output voltage and current. These four variables can be related by various equations, depending upon which variables are considered to be independent and which are dependent.

The *hybrid parameter* (h-parameter) equation pair (and its equivalent circuit) is often used for BJT circuit analysis. The equation pair is specified as follows:

$$v_1 = h_{11}i_1 + h_{12}v_2 \tag{3.2}$$

$$i_2 = h_{21}i_1 + h_{22}v_2 \tag{3.3}$$

The first digit of the subscript on h denotes the dependent variable and the second digit denotes the independent variable associated with the particular h-parameter. Hence, for example, h_{12} relates v_2 to v_1. The values of h are assumed to be constants.

When h-parameters are used to describe a transistor network, the equation pair is written as follows:

$$v_1 = h_i i_1 + h_r v_2 \tag{3.4}$$

$$i_2 = h_f i_1 + h_o v_2 \tag{3.5}$$

where the h-parameters are defined as follows:

$h_i = h_{11}$ = input resistance of transistor
$h_r = h_{12}$ = reciprocal voltage gain of transistor
$h_f = h_{21}$ = forward current gain of transistor
$h_o = h_{22}$ = output conductance of transistor

When h-parameters are applied to transistor networks, the parameters take on a practical significance as related to the transistor performance. The circuit developed using the h-parameters is shown in Figure 3.2. A simple application of Kirchhoff's laws to the circuit of Figure 3.2 shows that it satisfies equation (3.4) and equation (3.5).

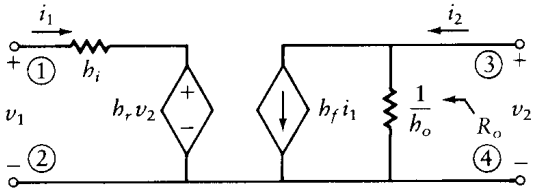


Figure 3.2
Equivalent circuit for h-parameters.

When the input and output parameters are individually set equal to zero, each hybrid parameter either represents a resistance, a conductance, a ratio of two voltages, or a ratio of two currents. The following equations are derived from equations (3.4) and (3.5). Following each equation are the units associated with the parameter and the name given to it.

$$R_{in} = h_i = \left.\frac{v_1}{i_1}\right|_{v_2=0}$$

ohms: short-circuit input **resistance with** v_2 shorted

$$h_f = \left.\frac{i_2}{i_1}\right|_{v_2=0}$$

dimensionless: forward current gain with v_2 shorted

$$h_r = \left.\frac{v_1}{v_2}\right|_{i_1=0}$$

dimensionless: **reverse** voltage gain with i_1 open circuited

$$Y_{out} = h_o = \left.\frac{i_2}{v_2}\right|_{i_1=0}$$

siemens (formerly mhos): **output conductance** with i_1 open-circuited

Although these parameters are ideally constant, the numerical values depend upon the transistor configuration. Thus, for example, if terminal 1 in Figure 3.2 is the base, 2 is the emitter and 3 is the collector, the circuit represents a CE configuration. Similarly, the transistor can be modeled as a CB configuration if terminals 1, 2, and 3 are the emitter, base, and collector, respectively.

It is helpful to have a way to distinguish among the three wiring configurations, i.e., CE, CC, and CB. A second subscript is added to each hybrid parameter to provide this bookeeping distinction. Thus, for example, a CE circuit normally has h_i in the base circuit, and it is renamed h_{ie}. Similarly for the CB, h_i is renamed h_{ib}, and for the CC, it is named h_{ic}. The three values of this short-circuit input impedance are related to each other as

$$h_{ie} = (1 + \beta)h_{ib} \approx \beta h_{ib} = h_{ic} \tag{3.6}$$

Figure 3.3 shows a CE amplifier with two different equivalent circuits. Although the h-parameter model defines the second subscript as associated with the type of amplifier configuration, h_{ib} and h_{ie} are values of resistance that are based upon the operating point of the amplifier and the location of these resistances within the equivalent circuit. In this case, the subscripts have nothing to do with the amplifier configuration. The same concept is also applied to h_{fe}, which refers to β regardless of how the transistor is placed within the amplifier configuration.

In each equivalent circuit, we have made the (usually reasonable) simplification that $h_r = h_o = 0$. Figure 3.3(b) uses the CE model, where the transistor has been replaced by the circuit of Figure 3.2 with terminal 1 as the base, 2 as the emitter, and 3 as the collector. In Figure 3.3(c), the transistor is replaced

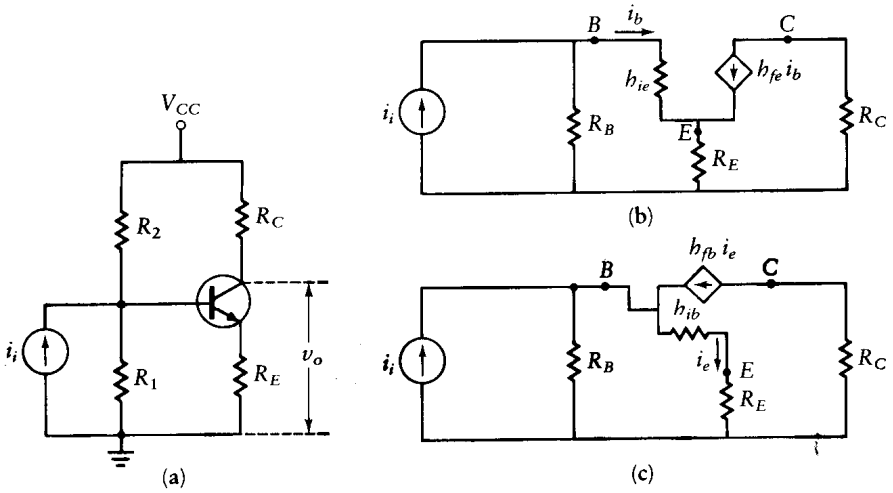


Figure 3.3
CE and equivalent circuits.

by the CB model. That is, using Figure 3.2, terminal 1 is the emitter, 2 is the base, and 3 is the collector.

For small-signal current, we see that h_{fe} is the ratio of the change in output current (Δi_C) to the change in input current (Δi_B). Recall that this relationship is also the defining expression for β. As a result,

$$h_{fe} = \beta = \left.\frac{\Delta i_C}{\Delta i_B}\right|_{v_{CE}=\text{constant}}$$

The actual value of β is a function of the operating point (I_{CQ}) of the transistor. In the flat portion of the i_C versus v_{CE} curve with i_B constant, there is little change in β. As the transistor approaches saturation, β starts dropping. As the transistor approaches cutoff, β also approaches zero.

Manufacturer's specifications often present a graph of h_{fe} as a function of i_C. The output conductance, h_o, of the transistor is usually small. Therefore, the output resistance, r_o, is usually large. As an example, let us examine the manufacturer's specification sheet for the 2N3903 (see Appendix D). It can be seen that the output conductance varies from 4 μS to 65 μS as i_C varies from 0.1 mA to 10 mA. This means that the output resistance varies from 15 kΩ to 250 kΩ. As an example of a typical value, when I_{CQ} is equal to 1 mA, the transistor output resistance is approximately 115 kΩ. With a typical load of 4 kΩ, the parallel combination is approximately 4 kΩ (since 115 kΩ is much larger than 4 kΩ) and r_o can be assumed to be infinite. The reverse voltage gain of the network, h_r, is also small and is ignored in the transistor equivalent circuit used in this text.

Another two-port model that is used in the study of transistor circuits is

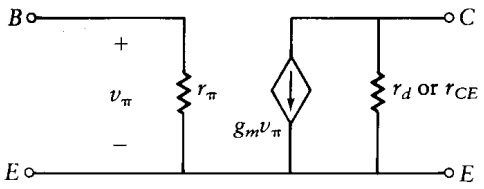


Figure 3.4
Hybrid-π model equivalent circuit.

the *hybrid-π* model, which is important when the transistor is used at high frequency. It includes the effects of parameters that become significant at high frequency (this is discussed in Chapter 10).

A low-frequency small-signal hybrid-π transistor model is shown in Figure 3.4. The model for low frequency is similar to that of the *h*-parameter model for the CE. The major difference is that the current-controlled current source of Figure 3.2 has been replaced by a voltage-controlled current source. In fact, a comparison of the parameters is easily accomplished as follows:

$$g_m = \frac{1}{h_{ib}}$$

$$r_\pi = h_{ie}$$

$$r_{CE} = \frac{1}{h_o}$$

3.2 Short-Circuit Input Resistance

We explore the parameter values before discussing the actual use of equivalent circuits for design and analysis. We first develop equations for h_{ie} and h_{ib}, which display the dependence of these parameters upon the location of the operating point.

We begin with the equation for the operating characteristics of the base-emitter junction, which acts as a diode, as presented in Chapter 1.

$$i_B = I_o \left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right]$$

This equation is now differentiated with respect to v_{BE} to obtain

$$\frac{di_B}{dv_{BE}} = \frac{I_o}{V_T} \exp\left(\frac{v_{BE}}{V_T}\right)$$

In the forward-bias region, i_B is approximately given by

$$i_B = I_o \exp\left(\frac{v_{BE}}{V_T}\right)$$

Then

$$\frac{di_B}{dv_{BE}} = \frac{i_B}{V_T}$$

But from the definition of h_{ie}, we obtain (see Figure 3.2)

$$h_{ie} = \left.\frac{\Delta v_1}{\Delta i_1}\right|_{v_2=0} = \frac{dv_{BE}}{di_B} = \frac{V_T}{I_{BQ}}$$

Now recall that

$$h_{ib} = \frac{h_{ie}}{\beta}$$

Finally,

$$h_{ib} = \frac{V_T}{|\beta I_{BQ}|} = \frac{V_T}{|I_{CQ}|} \tag{3.7}$$

Equation (3.7) is known as the *Shockley equation*. Using the approximation $V_T = 26$ mV, which applies to the BJT, equation (3.7) becomes

$$h_{ib} = \frac{0.026\ \text{V}}{|I_{CQ}|} \tag{3.8}$$

Equation (3.8) is useful in estimating the value of h_{ib} to be used in the equivalent circuit of Figure 3.3(c) (or g_m in the equivalent circuit of Figure 3.4).

3.3 CE Parameters

The equations that define ac amplifier parameters are summarized in Table 3.1 and are derived in the following sections. Note that the table gives two defining equations for each parameter. These are designated as the *long form*

and the *short form*. The short-form equation is a simplified version of the long-form equation and is derived by making assumptions about the relative sizes of some of the parameters. We point out the required assumptions as each equation is derived and the assumptions are in the table.

This double set of equations is used as the basis for our problem-solving technique. In general, we use the short-form equation because the parameters are not known more accurately. Then we verify that the assumptions necessary to make this short form valid do, in fact, hold. If short-form conditions apply, the component values are within the manufacturing tolerances. If short-form conditions do not apply, the calculations must be repeated using the long form equations.

Table 3.2 summarizes the equivalent circuits used in the derivations.

3.3.1 *Input Resistance, R_{in}*

The hybrid parameter circuit is used to derive the input resistance equation for each type of amplifier configuration. Figure 3.5 modifies the CE amplifier of Figure 3.3 by adding a capacitor-coupled load resistance. The basic circuit is shown in Figure 3.5(a), and two forms of equivalent circuit are shown in Figure 3.5(b) and (c). Note that we have omitted the reverse voltage gain, h_r, and the output admittance, h_o, from the model.

The equivalent circuit of Figure 3.5(b) is used to derive the input resistance, R_{in}. Usually β is large enough that we can approximate $1 + \beta$ as β. The current in R_E is therefore approximately equal to βi_b. If the circuit is now split as in Figure 3.5(c), the current through the resistor in series with h_{ie} in the input loop is i_b. Thus, to keep the voltage at the same value existing in the original circuit, we must change the resistor value to βR_E. The input resistance is then found by writing KVL and KCL equations for the input loop.

$$R_{in} = \frac{v_i}{i_{in}} = R_B \parallel (h_{ie} + \beta R_E) = \frac{R_B(h_{ie} + \beta R_E)}{R_B + h_{ie} + \beta R_E} \tag{3.9}$$

We substitute $h_{ie} = \beta h_{ib}$ to obtain

$$R_{in} = \frac{R_B(h_{ib} + R_E)}{R_B/\beta + h_{ib} + R_E} \tag{3.10}$$

If R_B is negligible compared to βR_E, equation (3.10) can be further simplified to the form given in equation (3.11).

$$R_{in} \approx \frac{R_B(h_{ib} + R_E)}{h_{ib} + R_E} = R_B \tag{3.11}$$

Table 3.1 Formula for Different Amplifier Configurations

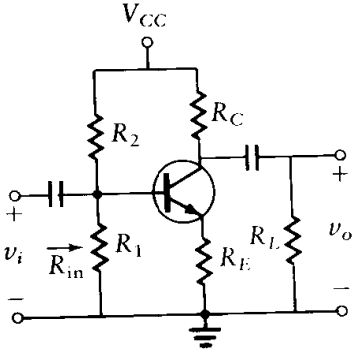
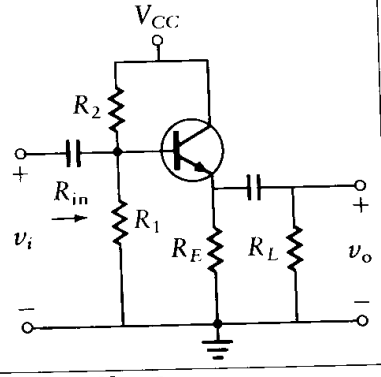
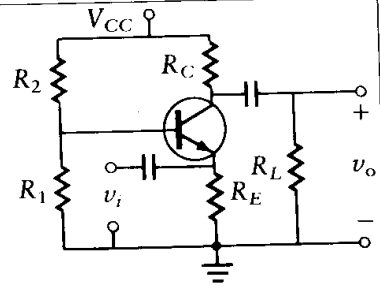
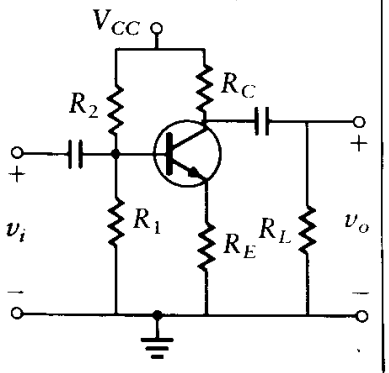
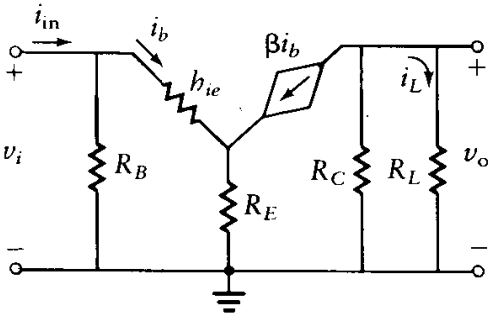
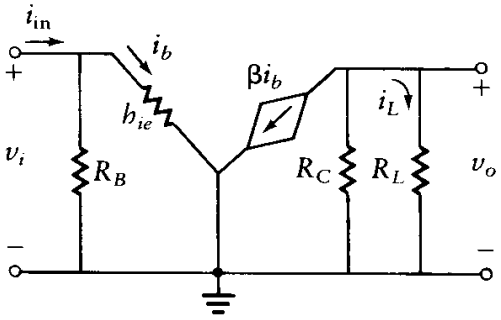
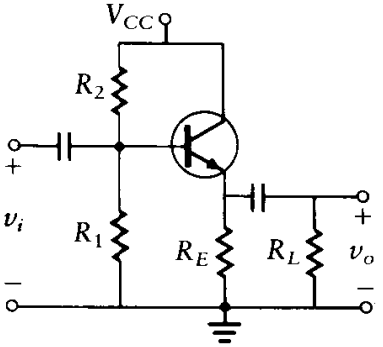
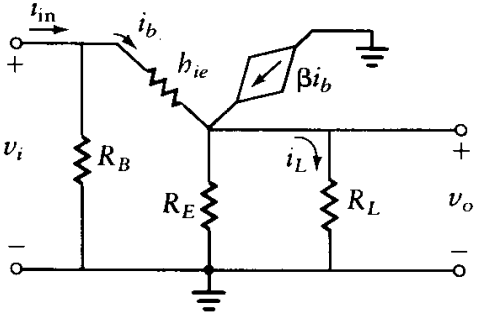
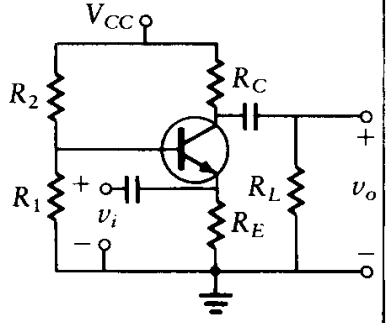
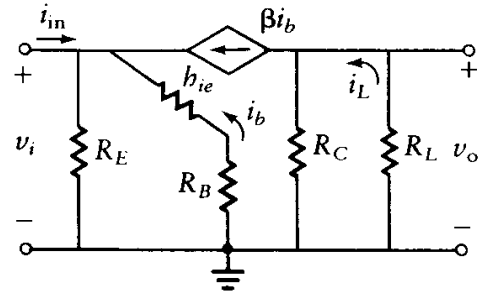
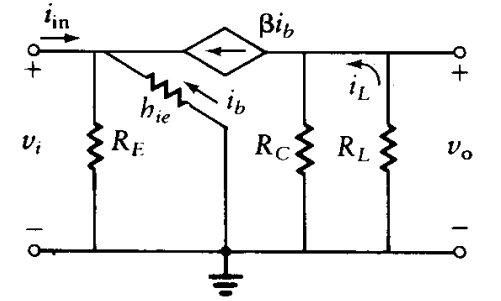
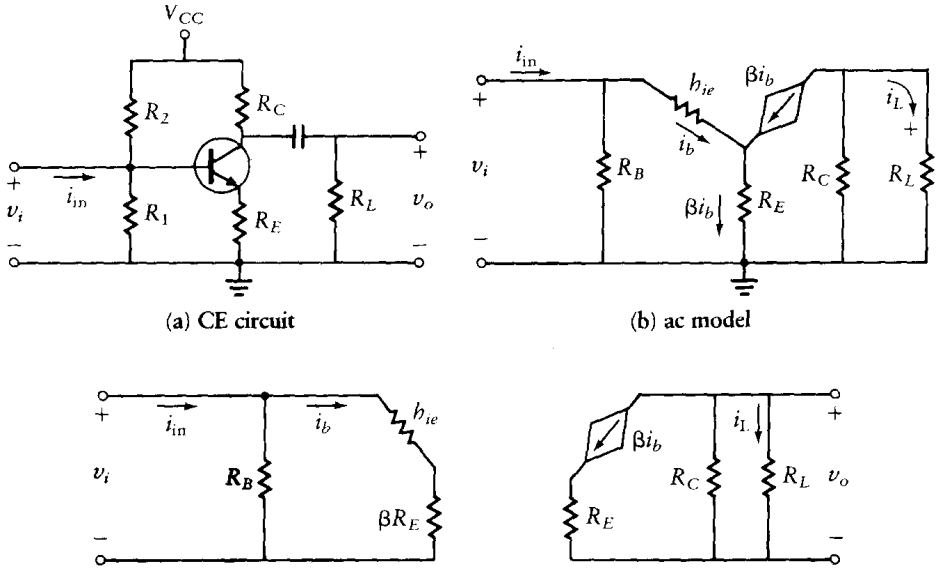
Type		Voltage Gain (A_v)	Current Gain (A_i)	Input Resistance (R_{in})
Common emitter		Long forms: $\frac{-(R_L\|R_C)}{h_{ib} + R_E}$	$\frac{-R_B}{\frac{R_B}{\beta} + h_{ib} + R_E} \quad \frac{R_C}{R_L + R_C}$	$\frac{R_B\,(h_{ib} + R_E)}{\frac{R_B}{\beta} + h_{ib} + R_E}$
		Short forms, if $h_{ib} << R_E$ and $R_B << \beta R_E$: $\frac{-R_L\|R_C}{R_E}$	$\frac{-R_B}{R_E} \frac{R_C}{R_C + R_L}$	R_B
Common collector (Emitter follower)		Long forms: $\frac{R_E\|R_L}{h_{ib} + (R_E\|\| R_L)}$	$\frac{R_B}{\frac{R_B}{\beta} + h_{ib} + (R_E\|R_L)} \frac{R_E}{R_E + R_L}$	$\frac{R_B\,[h_{ib} + (R_E\|R_L)]}{\frac{R_B}{\beta} + h_{ib} + (R_E\|R_L)}$
		Short forms, if $h_{ib} << R_E\|R_L$ and $R_B << (R_E \,\|\, R_L)\beta$: 1	$\frac{R_B}{R_L}$	R_B
Common base		Long forms: $\frac{R_C\|R_L}{h_{ib} + \frac{R_B}{\beta}}$	$\frac{+R_C}{R_C + R_L} \frac{R_E}{R_E + h_{ib} + \frac{R_B}{\beta}}$	$R_E\|(h_{ib} + \frac{R_B}{\beta})$
		Short forms, if $h_{ib} << R_E$ and $R_B << \beta R_E$: $\frac{R_C\|R_L}{h_{ib} + \frac{R_B}{\beta}}$	$\frac{R_C}{R_C + R_L}$	$h_{ib} + \frac{R_B}{\beta}$

Table 3.2 Equivalent Circuits for Different Amplifier Configurations

Type	Circuit	Equivalent Circuit	Equivalent Circuit with R_E Bypassed
Common emitter			
Common collector			
Common base			With R_B bypassed 



(a) CE circuit

(b) ac model

(c) Input and output separated

Figure 3.5
CE configuration.

Equation (3.10) is the long-form equation and it requires only one approximation, that is, $\beta >> 1$. Equation (3.11) is the short-form equation because it requires the additional approximation that $R_B << \beta R_E$, often expressed as $R_B \leq 0.1\ \beta R_E$.

3.3.2 *Voltage Gain, A_v*

The voltage gain is found from the definition

$$A_v = \frac{v_o}{v_i} = \frac{i_L R_L}{v_i}$$

The current-division relationship applied at the output of Figure 3.5(b) yields

$$i_L = \frac{-R_C \beta i_b}{R_L + R_C}$$

The negative sign results from the opposite direction of βi_b with respect to i_L. Then

$$A_v = -\frac{\beta R_L i_b}{v_i} \quad \frac{R_C}{R_L + R_C}$$

We wish to obtain an expression for A_v that does not contain other variables.

That is, we need to eliminate i_b and v_{in} from the above equation. Applying current division at the input yields the following expression for i_b:

$$i_b = \frac{R_B i_{in}}{R_B + h_{ie} + \beta R_E}$$

We then substitute this into the equation for A_v to obtain

$$A_v = \frac{-\beta R_L}{v_i} \quad \frac{R_C}{R_L + R_C} \quad \frac{R_B i_{in}}{R_B + h_{ie} + \beta R_E}$$

Since $v_i = i_{in} R_{in}$, we have

$$A_v = \frac{-\beta R_L}{i_{in} R_{in}} \quad \frac{R_C}{R_L + R_C} \quad \frac{R_B i_{in}}{R_B + h_{ie} + \beta R_E}$$

The i_{in} cancels from numerator and denominator. Since the parameter R_{in} is solved for in terms of transistor parameters and circuit elements, we can simplify this further. Substituting R_{in} from equation (3.9), we obtain

$$A_v = \frac{-\beta R_L R_C}{R_L + R_C} \quad \frac{R_B}{R_B + h_{ie} + \beta R_E} \quad \frac{R_B + h_{ie} + \beta R_E}{R_B(h_{ie} + \beta R_E)}$$

When like terms are canceled from the numerator and denominator and we recognize $h_{ie} = \beta h_{ib}$, this expression simplifies to the long form given in equation (3.12):

$$A_v = \frac{-\beta(R_L \parallel R_C)}{h_{ie} + \beta R_E} = \frac{-R_L \parallel R_C}{h_{ib} + R_E} \tag{3.12}$$

If $h_{ib} << R_E$, the equation further reduces to the short form given by equation (3.13):

$$A_v = \frac{-(R_L \parallel R_C)}{R_E} \tag{3.13}$$

If R_E is bypassed with a large capacitor so that the ac impedance is small, h_{ib} is no longer much less than R_E and the long form of equation (3.12) must be used. This becomes

$$A_v = \frac{-(R_L \parallel R_C)}{h_{ib}}$$

We can combine this with the h_{ib} approximation of equation (3.8) to obtain

$$A_v = \frac{-(R_L \parallel R_C)I_{CQ}}{0.026}$$

which shows that with R_E bypassed, the voltage gain of the amplifier is dependent upon the value of I_{CQ}.

3.3.3 *Current Gain, A_i*

The current gain is found from the gain impedance formula, equation (3.1).

$$A_i = \frac{R_{\text{in}}A_v}{R_L}$$

Substituting for A_v and R_{in} from equations (3.9) and (3.12), we obtain the long-form current gain of equation (3.14):

$$A_i = -\frac{R_B(h_{ie} + \beta R_E)}{(R_B + h_{ie} + \beta R_E)R_L}\frac{\beta(R_L \parallel R_C)}{h_{ie} + \beta R_E}$$

$$= -\frac{R_B R_C}{(R_B/\beta + h_{ib} + R_E)(R_C + R_L)} \tag{3.14}$$

If $R_B << \beta R_E$ and $h_{ib} << R_E$, the current gain simplifies to the short-form expression of equation (3.15):

$$A_i = -\frac{R_B R_C}{R_E(R_L + R_C)} \tag{3.15}$$

These equations for the CE amplifier are summarized in Table 3.1.

3.3.4 *Output Resistance, R_o*

In the equivalent circuit for the transistor, as shown in Figure 3.2, the output circuit contains an ideal current generator in parallel with a resistance of value $1/h_o$. The ideal current source exhibits an infinite impedance, since we measure output resistance with the input open circuited (i.e., $i_b = 0$). The output resistance for the CE transistor is then

$$r_o = \frac{v_2}{i_2} = \frac{1}{h_{oe}}$$

The parameter h_{oe} is usually small enough to be neglected in calculations, so the output resistance of the transistor becomes infinite in magnitude. The value of h_{oe} can be determined by consulting the transistor specifications. The output resistance, R_o, of a CE amplifier is the value of R_C when r_o is large. Most junction transistors typically have an r_o in excess of 50 kΩ.

Example 3.1 Capacitor-Coupled CE Amplifier (Design)

Design a CE amplifier (see Figure 3.6) with $A_v = -10$, $\beta = 200$ and $R_L = 1$ kΩ. A *pnp* transistor is used and maximum symmetrical output swing is required.

SOLUTION Refer to Figure 3.7 during this derivation. In Section 2.9.2 we learn how to select R_1 and R_2 for maximum symmetrical output swing when the other circuit parameters are known. The only additional information provided here is the value of A_v, yet there are two additional unknowns, R_C and R_E. Thus, we need another equation. We shall choose the other equation to force $R_C = R_L = 1$ kΩ (see Problem 3.17 for justification). We first try using the short-form equation for A_v in order to solve for R_E:

$$A_v = \frac{-(R_L \parallel R_C)}{R_E}$$

When known values are substituted into this equation, we find $R_E = 50\ \Omega$. We need to find h_{ib} in order to see if use of the short-form equation is justified. We first find R_{ac} and R_{dc} and then calculate the Q-point as follows:

$$R_{ac} = R_E + R_C \parallel R_L = 550\ \Omega$$

$$R_{dc} = R_E + R_C = 1050\ \Omega$$

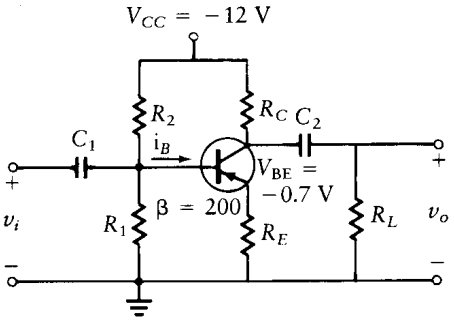


Figure 3.6
CE amplifier.

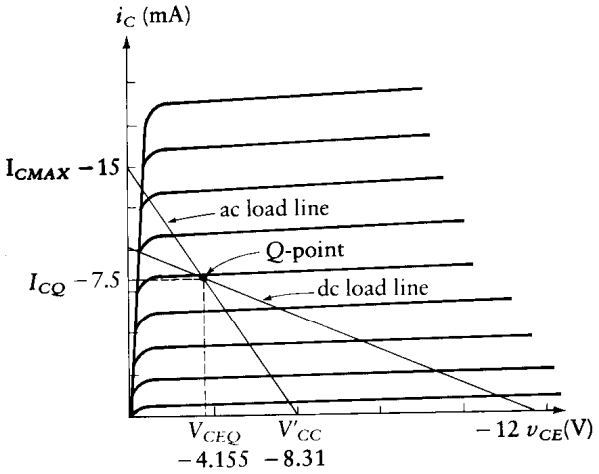


Figure 3.7
Load lines for Example 3.1.

With R_{ac} and R_{dc} determined, the design of this circuit now parallels the step-by-step procedure for ac design given in Section 2.9.2. The first step is to calculate the quiescent collector current needed to place the Q-point in the center of the ac load line (i.e., maximum swing). The equation is

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = -7.5 \text{ mA}$$

We now test the validity of the short-form equation for A_v. The quantity h_{ib} is found from equation (3.8) as follows:

$$h_{ib} = \frac{26 \text{ mV}}{|I_{CQ}|} = \frac{26 \text{ mV}}{7.5 \text{ mA}} = 3.47 \ \Omega$$

Then

$$R_E = 50 \ \Omega - h_{ib} = 46.5 \ \Omega$$

Since h_{ib} is much less than R_E, the short-form equation is valid, and we continue with the design.

If there were a current gain or input resistance specification for this design, we would use it to solve for the value of R_B. Since there is no such specification, we use the expression

$$R_B = 0.1 \ \beta R_E = 0.1(200)(50) = 1 \text{ k}\Omega$$

Because we are, in effect, forcing R_B to be less than βR_E by a factor of 10, the short form expression for A_i is probably valid. Therefore,

$$A_i = \frac{-R_B R_C}{R_E(R_C + R_L)} \approx \frac{-1000 \times 1000}{50 \times 2000} = -10$$

We now check this result by recalculating the current gain using the long form. We have

$$R_B = 0.1\,\beta R_E = 0.1(200)(46.5) = 930\ \Omega$$

Then

$$A_i = \frac{-R_B}{R_B/\beta + h_{ib} + R_E} \frac{R_C}{R_C + R_L} = -8.5$$

This shows that using the short-form expression results in an error greater than 10%. We therefore abandon the short form and continue using the long form expressions as follows:

$$V_{CEQ} = V_{CC} - (R_C + R_E)I_{CQ}$$

$$= -12 - (1046)(-0.0075) = -4.155\ \text{V}$$

$$V_{BB} = I_{CQ}\left(R_E + \frac{R_B}{\beta}\right) + V_{BE}$$

$$= (-0.0075)\left(46.5 + \frac{930}{200}\right) + (-0.7) = -1.08\ \text{V}$$

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{930}{1 - 1.08/12} = 1.02\ \text{k}\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{(930)(-12)}{-1.08} = 10.3\ \text{k}\Omega$$

$$R_{\text{in}} = \frac{R_B(h_{ib} + R_E)}{R_B/\beta + h_{ib} + R_E} = \frac{930(50)}{930/200 + 50} = 851\ \Omega$$

$$R_o = R_C = 1\ \text{k}\Omega \qquad \text{(assuming } r_o \text{ is large compared to } R_C\text{)}$$

The maximum peak-to-peak output swing is given by

$$2\,|I_{CQ}|\,(R_C \parallel R_L) = 2(.0075)(500) = 7.5\ \text{V}$$

The power delivered into the load and the maximum power dissipated by the transistor are found using equations from Sections 2.9 and 2.11.

$$P_L = \frac{(I_{CQ})^2 R_L}{8} = 7 \text{ mW}$$

$$P_T = V_{CEQ} I_{CQ} = 30.9 \text{ mW}$$

The load lines for this circuit are shown in Figure 3.7. If R_{in} or A_i had been specified (instead of A_v), then the equation for R_{in} or A_i could be used to determine R_B. Next, the equation

$$R_B = 0.1 \beta R_E$$

could be used to solve for R_E. **Thus,**

$$R_E = \frac{R_B}{0.1\beta}$$

3.4 Nonlinearities of BJTs

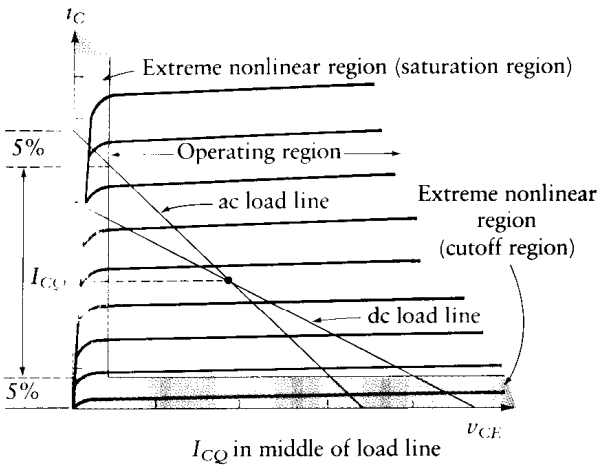
In Section 2.4.2, we learned that a transistor operates in a linear manner except in the saturation and cutoff regions. Operating in or near these regions causes distorted reproduction of an input signal. Therefore, the shaded regions shown in Figure 3.8 should be avoided. Designers frequently discard 5% of the characteristic curve in the vicinity of the saturation region and 5% of the curve near the cutoff region.

Using these guidelines and assuming the I_{CQ} has been placed in the center of the ac load line, the undistorted peak-to-peak output voltage is given by equation (3.16).

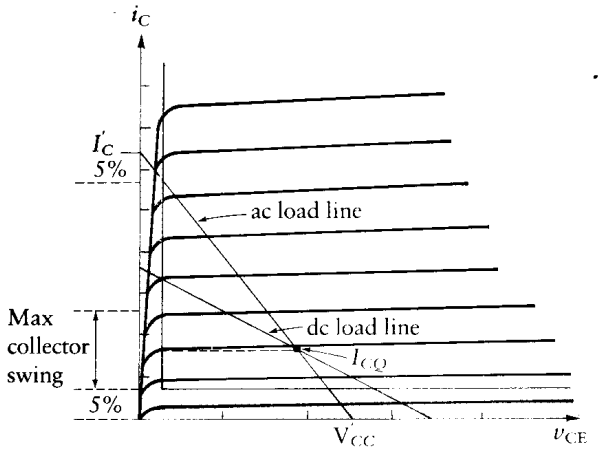
$$\begin{aligned} v_{o(p-p)} &= 0.9 \times 2 |I_{CQ}| (R_L \parallel R_C) \\ &= 1.8 |I_{CQ}| (R_L \parallel R_C) \end{aligned} \tag{3.16}$$

Suppose now that I_{CQ} is not in the middle of the load line. The circuit will have a reduced output swing for a symmetrical input signal. Figures 3.9(a) and (b) show this reduced swing graphically. The maximum symmetrical output swing can be determined as follows. Let us assume that the input is a sinusoid so that

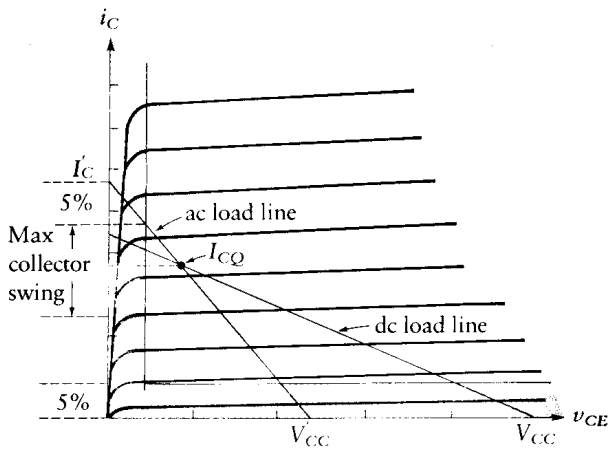
Figure 3.8
Nonlinear portions of characteristic curve.



I_{CQ} in middle of load line



(a) I_{CQ} below middle of ac load line



(b) I_{CQ} above middle of ac load line

Figure 3.9 Reduced swing on load line.

$$i_c(t) = I_{C\max}\sin \omega t$$

Then

$$v_o(\text{max undistorted swing}) = 2I_{C\max}(R_L \parallel R_C)$$

For the case where I_{CQ} is below the center of the ac load line as in Figure 3.9(a),

$$I_{C\max} = I_{CQ} - 0.05 \times I_C'$$

where, from Figure 3.9(a),

$$I_C' = \frac{V_{CC}'}{R_{ac}}$$

Then

$$v_o(\text{max undistorted swing}) = 2(I_{CQ} - 0.05I_C')(R_L \parallel R_C) \tag{3.17a}$$

For the case where I_{CQ} is above the center of the ac load line, as in Figure 3.9(b),

$$I_{C\,\max} = 0.95I_C' - I_{CQ}$$

Then

$$v_o(\text{max undistorted swing}) = 2(0.95I_C' - I_{CQ})(R_L \parallel R_C) \tag{3.17b}$$

Drill Problems

D3.1 The CE amplifier of Figure 3.5(a) has $V_{CC} = 15$ V, $R_L = \infty$, $V_{BE} = 0.7$ V, $R_C = 5$ kΩ, $R_E = 500$ Ω and $\beta = 200$. Determine R_1, R_2, A_v, A_i, and the maximum undistorted symmetrical output voltage when the Q-point is in the middle of the dc load line.

Ans.: $R_1 = 11.1$ kΩ; $R_2 = 104$ kΩ; $A_v = -10$;
$A_i = -20$; $v_{o(p-p)} = 12.2$ V

D3.2 In Problem D3.1, R_E is bypassed with a capacitor. What are the values of R_1, R_2, A_v, A_i, and R_o?

Ans: $R_1 = 11.1$ kΩ; $R_2 = 101$ kΩ; $A_v = -275$;
$A_i = -147$; $R_{in} = 2.67$ kΩ; $R_o = 5$ kΩ

D3.3 The *pnp* transistor amplifier shown in Figure 3.6 requires a voltage gain $A_v = v_o/v_i = -5$ and an input resistance, $R_{in} = 1$ kΩ. $R_L = 5$ kΩ, $V_{CC} = -12$V, $V_{BE} = -0.7$ V and $\beta = 200$. Determine the current gain, maximum output swing, and other resistor values.

Ans: $A_i = -1$; $v_{o\,\max} = 6.35$ V;
$R_1 = 1.1$ kΩ; $R_2 = 8.5$ kΩ

D3.4 Design a CE amplifier (Figure 3.6) with a voltage gain of $A_v = -60$, $R_L = 5$ kΩ and $R_{in} = 5$ kΩ. Design for the maximum voltage output swing.