TECHNICAL UNIVERSITY OF KOŠICE

FACULTY OF ELECTRICAL ENGINEERING AND INFORMATICS

DEPARTMENT OF ELECTRONICS AND MULTIMEDIA COMMUNICATIONS

BASIC OF ELECTRONICS

Lecture 4

2008/09

doc. Ing. Pavol Galajda, CSc.

Ing. Mária Gamcová, Ph.D.

Applied Informatics

Contents

References and Sources

[1] Attia, J. O.: *Electronics and Circuit Analysis using MATLAB*. CRC Press, Boca Raton London New York Washington, D.C., 1999.

[2] Fonstad, C. G: *Microelectronic Devices and Circuits.* McGraw-Hill Inc., New York, 1994.

[3] Galajda, P.– Lukáč, R.: *Elektronické prvky*. Merkury-Smékal, Košice, 2001.

[4] Galajda, P.– Lukáč, R.: *Elektronické obvody*. Merkury-Smékal, Košice, 2002.

[5] Rizzoni, G.*: Principles and Applications of Electrical Engineering,* 5th Edition. Ohio State University. McGraw-Hill Higher Education, 2007.

[6] Sandige, R.S.: *The Electrical Engineering Handbook*. Ed. Richard C. Dorf. Boca Raton: CRC Press LLC, 2000.

[7] Savant, C. J.– Roden, M. R – Carpenter, G. R.: *Electronic Circuit Design - An Engineering Approach*. The Benjamin/Cummings Publishing Company Inc., Menlo Park, California, 1987.

[8] Sedra, A. S.– Smith K. C.: *Microelectronic Circuits*. Oxford University Press, Inc., Oxford. New York, 1998.

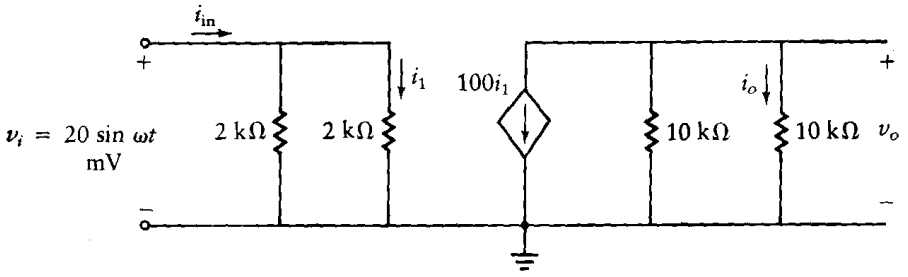


Figure 2.3
Solid-state equivalent circuit.

Then, using a current-divider relationship, the output current is found to be

$$i_o = \frac{10{,}000(-100i_1)}{10{,}000 + 10{,}000} = -50i_1$$

The voltage gain is

$$\frac{v_o}{v_i} = \frac{-5 \sin \omega t}{0.02 \sin \omega t} = -250$$

The current gain is

$$\frac{i_o}{i_{in}} = \frac{-50(10\ \mu A)}{20\ \mu A} = -25$$

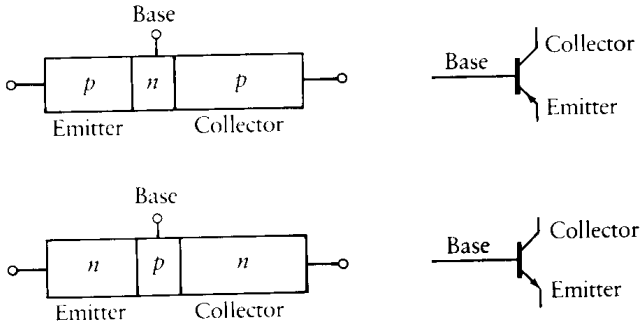
2.2 Bipolar Transistors

The transistor is a three-terminal device, in contrast to the diode, which is a two-terminal device. The diode consists of a *p*-type material and an *n*-type material; the transistor consists of two *n*-type materials separated by a *p*-type material (*npn* transistor) or two *p*-type materials separated by an *n*-type material (*pnp* transistor). Figure 2.4(a) illustrates the schematic representation of a transistor [22].

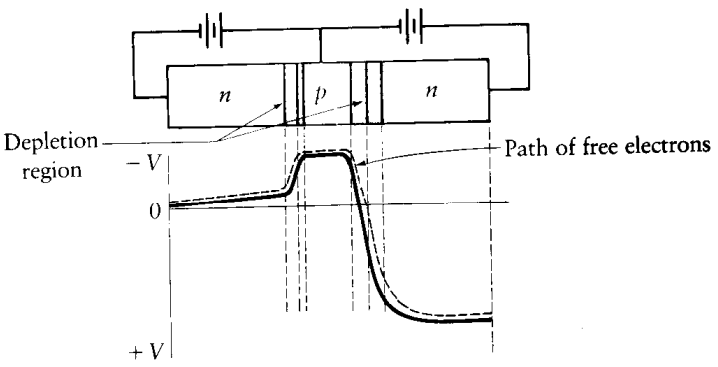
The three different layers or sections are identified as emitter, base, and collector. The *emitter* is a heavily doped, medium-sized layer designed to emit or inject electrons. The *base* is a medium doped, small layer designed to pass electrons. The *collector* is a lightly doped, large layer design to collect electrons.

The transistor can be idealized as two *pn* junctions placed back to back; these are called *bipolar junction transistors (BJTs)*.

In order to provide an explanation for the operation of the transistor, we



(a) Circuit **symbols**



(b) Potential-hill diagram

Figure 2.4
The bipolar transistor.

develop a simple mathematical model based upon the operational characteristics of the device for the region in which we are working. In order to keep the model simple, we confine our analysis to low frequencies. In Chapter 3 we modify our simple model to include input resistances. Then in Chapter 10, we expand the model to include additional components so that we can analyze transistor operation at high frequency.

The present model is sufficient to present concepts and to design for many useful low-frequency applications. It is intentionally kept uncomplicated so that a closed-form solution of the resulting equations is possible. If, however, more accurate results are required, computer analysis may be necessary. A computer-aided analysis program has been developed. It is known as *SPICE* (simulated program with integrated circuit emphasis; see Appendix A and [36], p. 254) and uses the *Gummel-Poon* model ([16], p. 286). Many U.S. companies use SPICE to develop multitransistor circuits and also for the purpose of doing "worst-case" analysis of circuits to determine the effects of component tolerance.

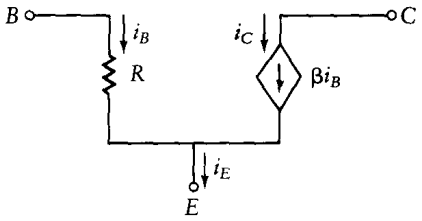
Models similar to the Gummel-Poon model as used in SPICE are discussed in Chapter 10, where high-frequency analysis and design are considered.

2.3 Transistor Operation

A simple but effective explanation of the *npn* transistor operation is developed using the potential-hill diagram technique of Figure 2.4(b). This approach illustrates a simplified visual picture of the basic operation of a bipolar transistor so that simple circuit applications can be understood. When the base-emitter junction is biased in the forward direction and the base-collector junction is biased in the reverse direction, electrons leaving the *n*-material of the emitter will see only a small potential hill at the *np* junction. Since the potential hill is small, most of the electrons have enough energy to progress to the top of the hill. Once on top of the potential hill, the electrons move easily through the *p*-material (base) to the *pn*- (base-collector) junction. When they approach that junction, the electrons are under the influence of the positive supply voltage and move forward rapidly as they move down the potential hill. If the forward bias on the base-emitter junction is reduced, the height of the potential hill is raised. Electrons leaving the emitter will have more difficulty in reaching the top. The electrons reaching the top are the ones with the highest amount of energy, and these will progress to the collector. The reduction of forward bias thus causes the current through the transistor to be considerably reduced. On the other hand, increasing the forward bias on the base-emitter junction will reduce the potential hill and allow more emitter electrons to flow through the transistor.

The current flow in a junction transistor can also be understood by examining charge-carrier behavior and the depletion regions. The depletion regions have been indicated on Figure 2.4(b). Note that since the base-emitter junction is forward-biased, the depletion region is relatively narrow. The reverse is true for the base-collector junction. A large number of majority carriers (electrons) will diffuse across the base-emitter junction, since this is forward-biased. These electrons then enter the base region and have two choices. They may either exit this region through the connection to the voltage sources, or they may continue flowing to the collector region across the wide depletion region of the reverse-biased junction. We would normally expect the major portion of this current to return to the source, except for the following observations. Since the base region is so thin, these electrons need to travel less distance to be attracted to the positive potential of the collector connection. In addition, the base material has a low conductivity, so the path to the source lead represents a high impedance path. In reality, a very small fraction of the electrons leave the base through the source connection—the major portion of current does flow into the collector.

The bipolar junction transistor exhibits a current gain, which can be used to amplify signals. A simplified *npn* transistor equivalent circuit is shown in



i_B = base current
i_C = collector current
i_E = emitter current
R = resistance between base and emitter

Figure 2.5
Simplified transistor equivalent circuit.

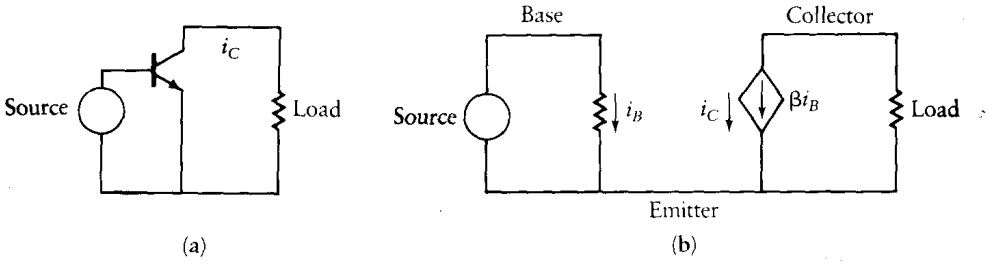


Figure 2.6
Simple transistor circuit.

Figure 2.5. This model is usually adequate for design and analysis of most circuits.

Figure 2.6 shows a simple circuit for producing current gain. A source voltage is applied across the base-emitter, and a load resistance is connected between the collector and emitter. Figure 2.6(b) shows the same circuit, where the transistor is replaced by the model of Figure 2.5. Because of the presence of the dependent source, a current in the base lead controls the current from the collector to the emitter. The collector current source is dependent upon the base current, i_B. As i_B is increased, the collector current, i_C, increases proportionally. The proportionality constant is given the name *beta* (β).

Figure 2.7 shows a refined version of this model, known as the *Ebers-Moll model* [32]. The base-emitter junction acts as a forward-biased diode with a forward current of $i_B + i_C$. The base-collector junction is reverse-biased and exhibits a small leakage current. I_{CBO}, and a larger current, βi_B. This latter current is caused by the interaction of currents in the base. Clearly,

$$i_E = i_C + i_B \tag{2.1}$$

Note that the positive direction of base and collector currents are defined to be *into* the transistor, whereas the reverse is true for the emitter current. This is simply a convention, and we could have just as well reversed any of the directions. The Ebers-Moll model includes a current, I_{CBO}, which is independent of the base current.

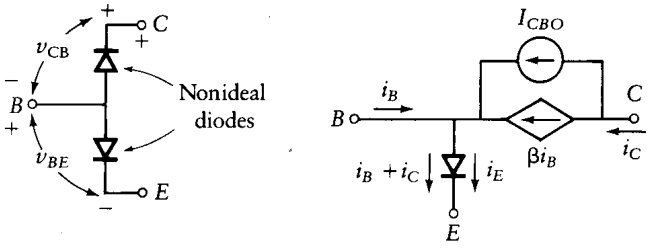
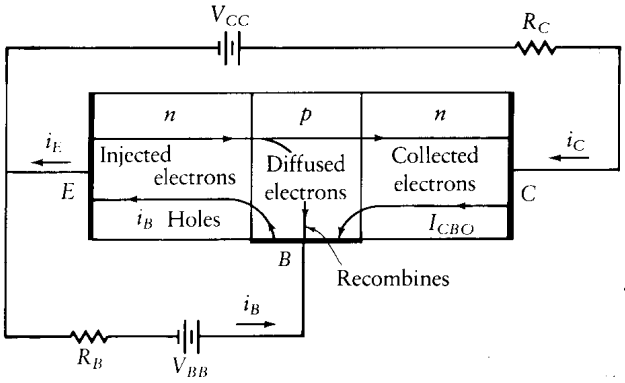
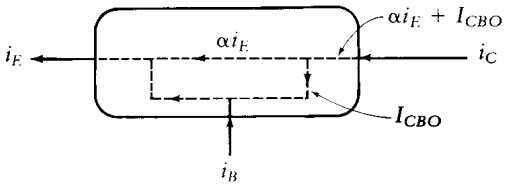


Figure 2.7
Ebers-Moll model.



(a) Detailed inside view



(b) Simplifed view

Figure 2.8
Internal currents in a transistor.

The *common-base current gain,* α, is defined as the ratio of the change in collector current to the change in emitter current, assuming that the voltage between collector and base is a constant. Thus,

$$\alpha = \left.\frac{\Delta i_C}{\Delta i_E}\right|_{v_{CB}=\text{constant}}$$

This is shown pictorially in Figure 2.8 where I_{CBO} is the leakage current between base and collector. We wish to find a relationship between the collector and base currents. The collector current is found by viewing Figure 2.8(b):

$$i_C = \alpha i_E + I_{CBO} \tag{2.2}$$

Combining equation (2.1) with equation (2.2) yields the emitter current,

$$i_E = \alpha i_E + I_{CBO} + i_B$$

and solving for the base current,

$$i_B = i_E(1 - \alpha) - I_{CBO} \tag{2.3}$$

We can eliminate i_E from equation (2.3) by rewriting equation (2.2) as

$$i_E = \frac{i_C - I_{CBO}}{\alpha}$$

Finally, this is substituted in equation (2.3) to yield a relationship between i_B, i_C, and I_{CBO}:

$$\begin{aligned} i_B &= \frac{(i_C - I_{CBO})(1 - \alpha)}{\alpha} - I_{CBO} \\ &= \frac{(1 - \alpha)i_C}{\alpha} - \frac{I_{CBO}}{\alpha} \end{aligned} \tag{2.4}$$

The common-base current gain, α, usually lies in the range from 0.8 to 0.999. Therefore, the reciprocal can often be approximated as unity, thus yielding

$$i_B = \frac{(1 - \alpha)i_C}{\alpha} - I_{CBO}$$

Beta (β) was used earlier (see Figure 2.6) to define the ratio of changes in collector current to changes in base current. That is,

$$\beta = \frac{\Delta i_C}{\Delta i_B}$$

Therefore, we differentiate equation (2.4) and rearrange terms.

$$\beta = \frac{\alpha}{1 - \alpha}$$

Typical values of β range from 10 to 600. Making the substitution for β yields

$$i_B = \frac{i_C}{\beta} - I_{CBO}$$

We can usually neglect I_{CBO}, since it is small in magnitude. Thus,

$$i_C \approx \beta i_B \tag{2.5}$$

The term β is referred to as the *large-signal amplification factor,* or the *dc amplification factor.* Thus we are back to our original simplified model. In practice, the value of β varies with base current.

Design challenges exist because β varies with changes in the transistor current. Additionally, during the fabrication of the transistor, variation of the value of beta occurs within a single production run. Thus, two transistors fabricated at the same time will have different values of β, even at the same current levels. This leads us to develop a design procedure that makes the value of collector current relatively independent of changes in β. These methods are discussed in Section 2.5.

Another simplifying assumption often made is that the collector current is approximately equal to the emitter current. That is, since I_{CBO} is small compared to i_C and since α ranges from 0.9 to 0.999, we have

$$i_C \approx i_E \tag{2.6}$$

2.4 Transistor Circuits

2.4.1 *Common Circuit Configurations*

There are three general configurations utilized in transistor circuits. The most often used is the *common-emitter* (*CE*) *amplifier,* so called because the emitter is in both the input and output loops. The next most widely used circuit is the *common-collector* (*CC*) configuration, also known as the *emitter follower.* The third configuration is the *common-base* (*CB*) circuit. Examples of these amplifier configurations are shown in Figure 2.9, where we have illustrated the circuits using *npn* transistors.

In this chapter we consider the design of the bias, or dc circuit. This is characterized by the base resistor, R_B, the emitter resistor, R_E, the collector resistor, R_C, and the source voltage, V_{CC}. The bias technique for the CE amplifier is the same as that for the CB configuration, so these are considered together. The CC configuration is considered separately. When we use *pnp* transistors, the voltage polarities of V_{BB} and V_{CC} are reversed, but the ac equivalent circuits we have developed remain the same.

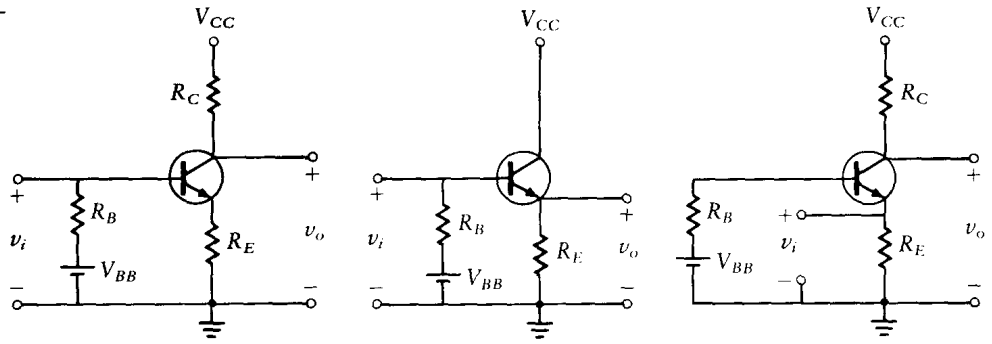


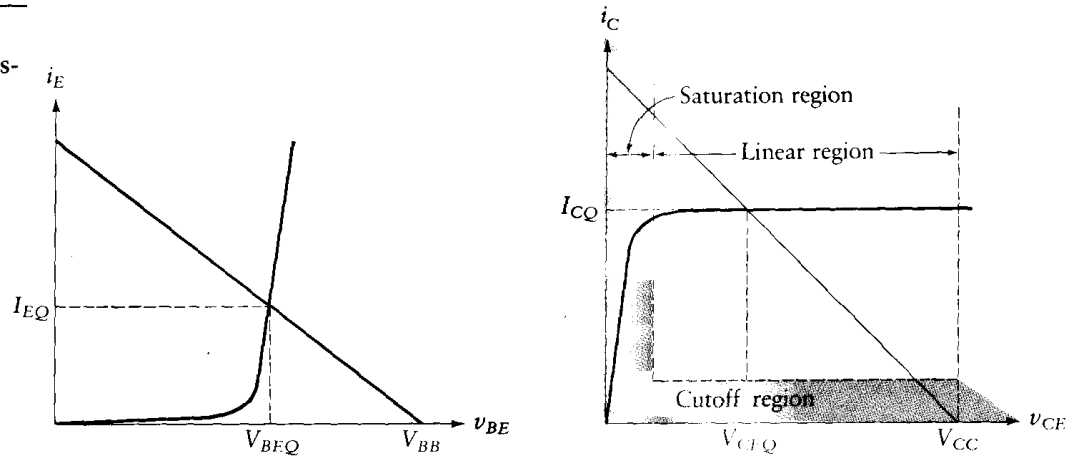
Figure 2.9
Amplifier circuits.

2.4.2 *Characteristic Curves*

Since the transistor is a nonlinear device, one way to define its operation is with a series of characteristic curves in a manner similar to that used for diodes in the previous chapter. There is a set of curves for each type of transistor. Since we are no longer dealing with two terminal devices, equations involve at least three variables. Therefore, *parametric curves* are usually used to describe transistor behavior. Figure 2.10 shows two typical plots. Figure 2.10(a) shows the emitter current as a function of the voltage between base and emitter when v_{CE} is held constant. Note that, as we might have expected, this curve is similar to the curve for a diode, since it is the characteristic of the current in the single junction. A load line is drawn using the two axis intercepts. When $i_E = 0$, $v_{BE} = V_{BB}$. The other intercept is found by setting $v_{BE} = 0$. The point where the load line crosses the i_E versus v_{BE} curve is called the *quiescent point,* or simply *Q-point.* The slope of the load line is $-1/(R_E + R_B)$. That is, the equivalent resistance seen by the base and emitter terminals is simply $R_E + R_B$. The slope of the characteristic curve is $1/r_d$, where r_d is the *dynamic resistance* of the transistor emitter-base junction. This slope can be calculated from equation (1.1) and the simplifications that follow that equation. Since this is a *pn* junction, $nV_T = 26$ mV (assuming a silicon junction at room temperature). Taking the derivative of equation (1.1) and performing appropriate simplifications, we find the dynamic resistance to approximately equal

$$r_d \approx \frac{0.026}{I_{EQ}}$$

where I_{EQ} is the emitter current at the Q-point.



(a) Emitter-base characteristics (b) Collector-emitter characteristics

Figure 2.10
Transistor characteristic curves.

Since $i_B = i_C/\beta$, the base-emitter junction is similar to that of a diode. Therefore, for the forward-biased junction,

$$i_B = \left(\frac{I_o}{\beta}\right) \exp\left(\frac{v_{BE}}{nV_T}\right)$$

For a silicon diode, n has a value of 1.3 to 1.6. However, in silicon transistors, the value of n has a value close to unity because of recombination effects caused by the collector and base currents combining in the emitter region. Diffused transistors exhibit an increase of 10 to 20% in the value of n for current levels above the normal operating range of the transistor. In this text, we use $n = 1$ and $nV_T = 26$ mV for silicon transistors.

A straight-line extension of the characteristic curve would intersect the v_{BE} axis at 0.7 V for silicon transistors, 0.2 V for germanium, and 1.2 V for gallium arsenide devices.

If we now hold i_B constant, the collector-emitter junction is defined by the curve of i_C versus v_{CE} shown in Figure 2.10(b). As can be seen from this typical curve, the collector current is almost independent of the voltage between the collector and the emitter, v_{CE}, throughout the "linear range" of operation. When i_B is close to zero, i_C approaches zero in a nonlinear manner. This is known as the *cutoff region* of operation. For the section of the characteristic curves where v_{CE} is near zero, i_C is maximum. This region, known as the *saturation region,* is also not usable for amplification because of nonlinear operation.

Transistor characteristic curves are parametric curves of i_C versus v_{CE}, where i_B is a parameter. Figure 2.11 shows an example of a family of such curves. Each transistor type has its own unique set of characteristic curves.

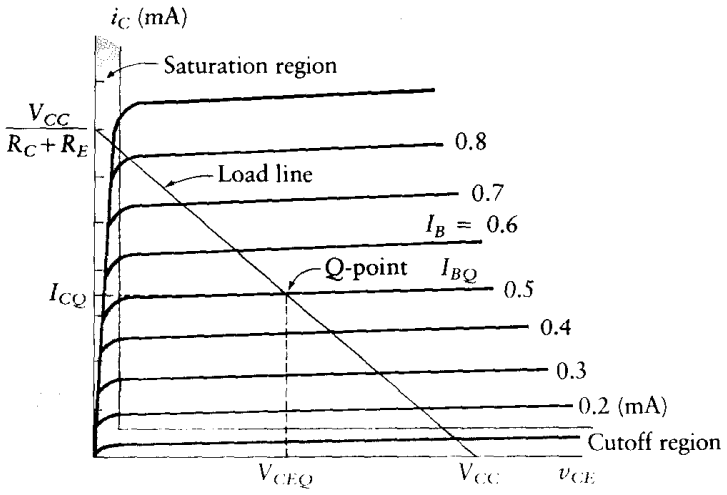


Figure 2.11 Family of transistor characteristic curves.

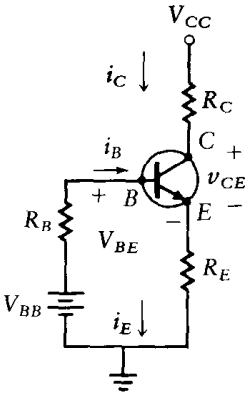


Figure 2.12 Simple transistor circuit.

As an example of the use of the characteristic curves, we shall analyze the circuit of Figure 2.12. Applying KVL around the collector to emitter loop, we obtain

$$V_{CC} = i_C R_C + v_{CE} + i_E R_E \tag{2.7}$$

Since i_E is approximately equal to i_C, equation (2.7) can be simplified, as in equation (2.8).

$$V_{CC} = i_C(R_C + R_E) + v_{CE} \tag{2.8}$$

Equation (2.8) defines a straight-line relationship between i_C and v_{CE}. That is,

$$i_C = \frac{V_{CC} - v_{CE}}{R_C + R_E} = -\frac{1}{R_C + R_E} v_{CE} + \frac{V_{CC}}{R_C + R_E} \tag{2.9}$$

One way to plot this straight line is to solve for the two axis intercepts. If $i_C = 0$, $v_{CE} = V_{CC}$. If $v_{CE} = 0$, then

The dc load line is plotted on the characteristic curves of Figure 2.11. When we discuss design, we will see how properly to select the circuit parameters. For now, we assume that the operating point, the Q-point, can be selected

anywhere on this load line. The point will have coordinates of V_{CEQ} and I_{CQ}, the quiescent values of v_{CE} and i_C, respectively. The quiescent point is the zero signal value of v_{CE} and i_C.

2.5 The CE Amplifier

The CE, or common emitter transistor amplifier, is so called because the base and collector current combine in the emitter. Figure 2.13 shows the configuration of the amplifier, where an *npn* transistor has been selected for illustration.

We first analyze the circuit of Figure 2.13 under dc conditions. The variable source, v_s, is set equal to zero. KVL around the base loop is written as follows:

$$I_B R_B + V_{BE} - V_{BB} = 0 \tag{2.10}$$

Recall that V_{BE} is equal to 0.6 to 0.7 V for silicon transistors, but in this text, we use 0.7 V unless otherwise specified.

We now write the KVL around the collector-emitter loop as follows:

$$V_{CC} = R_C I_C + V_{CE}$$

Then

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{2.11}$$

Equation (2.11) defines the load line, which is drawn on the characteristic curves in Figure 2.14(a). A Q-point, or operating point, which is defined as the zero-signal point, can now be selected to lie on the load line. Now if we assume an ac input of

$$v_s = V \sin \omega t$$

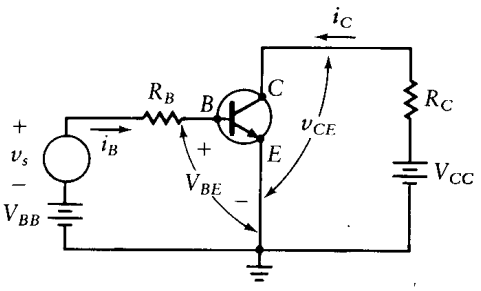
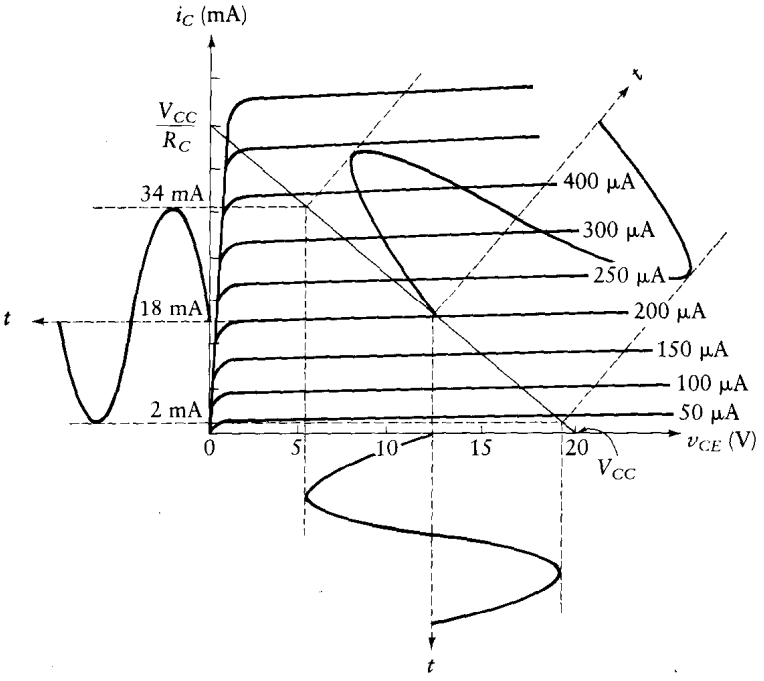
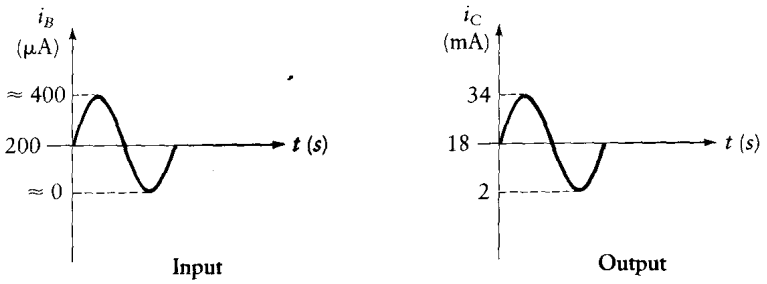


Figure 2.13
Common emitter *npn* transistor amplifier.



(a) Transistor characteristics curve



(b) Input-output current curves

Figure 2.14
Characteristic curves for CE amplifier.

the output wave can be found graphically. By moving the operating point up and down along the load line as i_B varies, we can plot i_C, i_B, and v_{CE}, as shown in Figure 2.14.

Let us determine the change in collector current for a given change in base current. This ratio is the *current gain,* which is defined as

$$A_i = \frac{\Delta i_C}{\Delta i_B}$$

$$= \frac{32 \text{ mA}}{400 \ \mu\text{A}} = 80$$

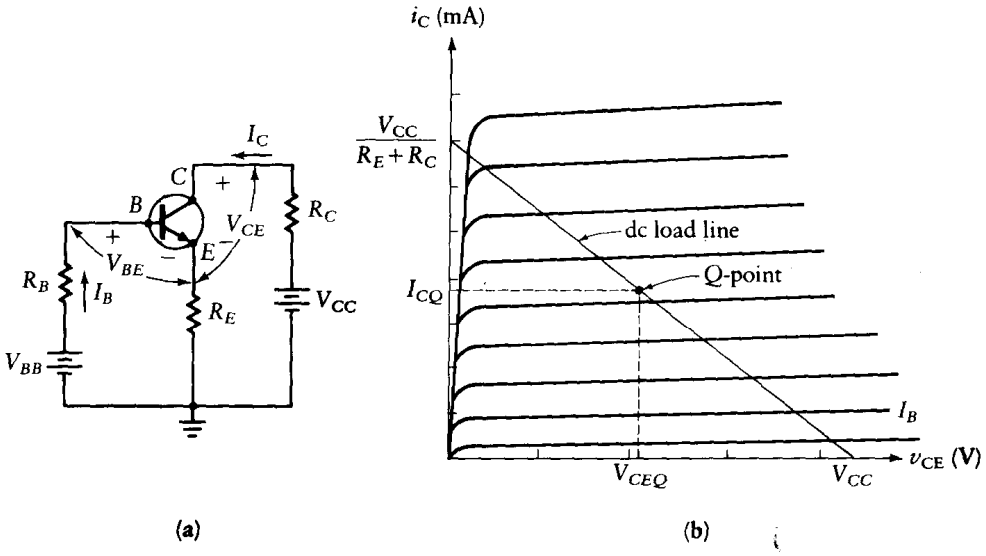


Figure 2.15
CE amplifier with emitter resistor.

Δi_C and Δi_B are read from Figure 2.14 as the total swings in these parameter values. It is this gain that makes the device important for many engineering applications.

2.5.1 *CE Amplifier with Emitter Resistor*

Figure 2.15 illustrates a CE circuit to which an emitter resistor has been added. We write the Kirchhoff equations around the emitter-collector loop to determine the dc load line. Referring to Figure 2.15(a), we find

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$

Since I_C is approximately equal to I_E, we have

$$I_C = \frac{V_{CC} - V_{CE}}{R_E + R_C} \tag{2.12}$$

If $I_C = 0$, then

$$V_{CE} = V_{CC}$$

This operating point is in the cutoff region. If $V_{CE} = 0$, we have

$$I_C = \frac{V_{CC}}{R_E + R_C}$$

This operating point is in the saturation region. The resulting load line is as drawn in Figure 2.15(b).

In using the common emitter transistor, we avoid the nonlinear region of the characteristic curves occurring at low values of i_C (cutoff) and at low values of v_{CE} (saturation). In designing a transistor amplifier, we often desire maximum undistorted output swing. If the ac input signal is symmetrical about zero, we can achieve maximum swing by placing the Q-point in the center of the load line. Thus,

$$V_{CEQ} = \frac{V_{CC}}{2}$$

This equation establishes V_{CEQ} and I_{CQ}. Additionally, since the base-emitter junction acts as a diode,

$$V_{BE} = V_\gamma$$

Writing KVL equations around the base loop, we obtain

$$V_{BB} = R_B i_B + v_{BE} + i_C R_E$$

Note that we are using lowercase letters and uppercase subscripts for the variables. This indicates total (dc + ac) values. This would be an appropriate time to review the notation conventions presented at the beginning of this text. Because

$$i_C = \beta i_B$$

we have

$$V_{BB} = \frac{R_B i_C}{\beta} + V_{BE} + i_C R_E$$

and at the quiescent point,

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} \tag{2.13}$$

The voltage, V_{BE}, is considered to be a constant at room temperature (25°C) and has a value of about 0.7 V for silicon transistors. In order to avoid using two separate dc sources, a voltage-divider network can be used to provide the dc source for the base circuit, as shown in Figure 2.16. The values for R_1 and

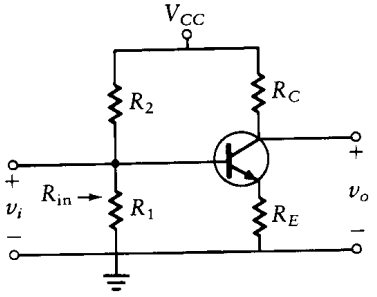


Figure 2.16
Transistor circuit using one source.

R_2 determine the location of the Q-point. If the resistor and source combination connected to the base in Figure 2.16 is replaced by a Thevenin equivalent, the new circuit is identical to that of Figure 2.15. Therefore, it is necessary only to properly choose R_1 and R_2.

The Thevenin equivalent voltage and resistance from base to ground are

$$V_{TH} = V_{BB} = \frac{R_1 V_{CC}}{(R_1 + R_2)} \tag{2.14}$$

$$R_{TH} = R_1 \parallel R_2 = R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{2.15}$$

We can **solve for R_1 and R_2 by substituting equation (2.14) into equation** (2.15):

$$R_1 = \frac{R_B V_{CC}}{V_{CC} - V_{BB}} = \frac{R_B}{1 - V_{BB}/V_{CC}} \tag{2.16}$$

$$R_2 = \frac{V_{CC} R_B}{V_{BB}} \tag{2.17}$$

R_1 and R_2 need to be determined to establish the required bias point. The analysis of the previous section assumes that the collector current is equal to the emitter current. This is a good approximation, since β is usually greater than 100.

For the circuit under consideration, we wish to have about 10% of the input current going into the base and about 90% shunted through the equivalent external resistor, R_B. This provides bias stability and also permits the use of the simplified equations. Hence, the current in R_B should be about 10 times the base current. To achieve this, we set

$$R_B \leq 0.1\, \beta R_E \tag{2.18}$$

or

$$\frac{R_B}{\beta} \leq 0.1R_E$$

This prevents variation in β from significantly affecting the dc operating point of the stage. We will have more to say about this later.

We can now use equation (2.13) to solve for the quiescent collector current. Letting R_B equal 0.1 βR_E, we have

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{0.1\ \beta R_E/\beta + R_E} = \frac{V_{BB} - V_{BE}}{1.1R_E} \tag{2.19}$$

Equation (2.19) is used in the design process.

2.5.2 *Introduction to Analysis and Design*

In *analysis* problems, the circuit is completely specified. Therefore the Q-point is known, since both R_1 and R_2 are given. The bias point may not be optimally located, and, in fact, we may find that the transistor is in the saturation or cutoff region. Nonetheless, since the entire circuit is specified, we can only substitute values into equations and calculate the results.

In *design* problems, the circuit is *not* completely specified. The designer has the option of placing the quiescent point in the best possible location. If it is desired to have the maximum possible output voltage swing, the Q-point is placed in the center of the load line. If, on the other hand, the input signal is small, I_{CQ} can often be set at a smaller value to obtain a linear (nondistorted) output, while dissipating less power in the rest condition. Since specification of the Q-point does not yield a sufficient number of equations to solve for all components, additional constraints can be introduced to provide performance improvement. For example, we use the equation $R_B = 0.1\ \beta R_E$ in order to find R_1 and R_2. Recall that choosing R_B according to this equation makes the Q-point location less sensitive to variations in β. Sometimes the circuit configuration will dictate other constraints upon the resistor values that will not permit satisfying this last relationship.

Example 2.1 Analysis of CE Amplifier

A CE amplifier is configured as shown in Figure 2.17 with $R_1 = 1$ kΩ, $R_2 = 9$ kΩ, $R_C = 1$ kΩ, $V_{CC} = 12$ V, $R_E = 100$ Ω, $\beta = 100$, and $V_{BE} = 0.6$ V. Determine V_{BB}, R_B, and I_{CQ}.

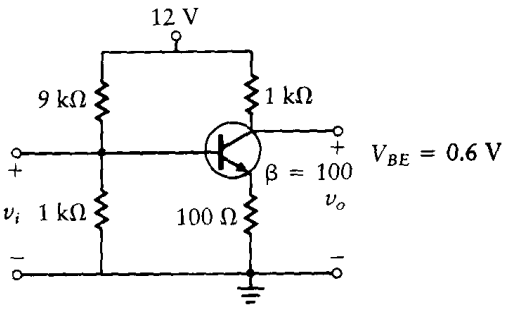


Figure 2.17
CE amplifier for Example 2.1.

SOLUTION We first find the Thevenin equivalent of the resistive network connected to the base.

$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2} = \frac{(1000)(12)}{(1000 + 9000)} = 1.2 \text{ V}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{(1000)(9000)}{(1000 + 9000)} = 900\ \Omega$$

We now use the KVL equation for the base loop, equation (2.13), to obtain

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} = \frac{1.2 - 0.6}{900/100 + 100} = 5.5 \text{ mA}$$

Example 2.2 Design of CE Amplifier

In the circuit of Figure 2.17, we wish to place the Q-point in the middle of the load line. Here, $\beta = 100$, $V_{BE} = 0.6$ V, $R_E = 100\ \Omega$, $R_C = 1$ kΩ, and $V_{CC} = 12$ V. Find the required values of R_1 and R_2.

SOLUTION The specification that the Q-point is in the middle of the load line requires that

$$V_{CEQ} = \frac{V_{CC}}{2}$$

We can then use KVL around the emitter-collector loop, equation (2.12), to find I_{CQ}:

$$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_E + R_C} = \frac{V_{CC} - V_{CC}/2}{R_E + R_C} = \frac{12}{2(100 + 1000)} = 5.5 \text{ mA}$$

We need to know R_B and V_{BB} in order to find R_1 and R_2. R_B is found from the constraint

$$R_B = 0.1\,\beta R_E = 0.1(100)(100) = 1\ \text{k}\Omega$$

We now use the base loop KVL equation, equation (2.13), to find V_{BB} as follows:

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E\right)$$
$$= 0.6 + (0.0055)\left(\frac{1000}{100} + 100\right) = 1.2\ \text{V}$$

With V_{BB} and R_B determined, equations (2.16) and (2.17) can be used to find R_1 and R_2.

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{1000 \times 12}{1.2} = 10\ \text{k}\Omega$$

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{1000}{1 - 1.2/12} = 1.11\ \text{k}\Omega$$

Drill Problems

D2.1 Given the circuit of Figure 2.16 with $V_{CC} = 16$ V, $R_1 = 2$ kΩ, $R_2 = 20$ kΩ, $R_C = 3$ kΩ, $R_E = 200$ Ω, $\beta = 200$, and $V_{BE} = 0.7$ V, determine the values of V_{BB}, R_B, and I_{CQ}.

Ans. 1.46 V; 1.82 kΩ, 3.6 mA

D2.2 Given the circuit of Figure 2.16 with a *pnp* transistor, $V_{CC} = -6$ V, $R_1 = 2$ kΩ, $R_2 = 12$ kΩ, $R_C = 1$ kΩ, $R_E = 100$ Ω, $\beta = 100$, and $V_{BE} = -0.7$ V, determine the values of V_{BB}, I_{CQ}, and R_B.

Ans. −0.86 V; −1.34 mA; 1.71 kΩ

D2.3 Given the circuit of Problem D2.1 but with R_1 and R_2 not specified, design a circuit for maximum output voltage swing. Determine the new values of R_1, R_2, and I_{CQ}.

Ans: 4.34 kΩ; 51.2 kΩ; 2.5 mA

D2.4 Using the information given in Problem D2.2, design a circuit for maximum output voltage swing. Determine the new values of R_1, R_2, and I_{CQ}.

Ans: 1.2 kΩ; 6 kΩ; −2.73 mA

D2.5 In the amplifier of Problem D2.1, R_B is required to be 10 kΩ. What are the values of R_1, R_2, I_{CQ}, and R_E that make the amplifier operate with maximum output voltage swing and insensitivity to variations in β?

Ans: 11.4 kΩ; 81.8 kΩ; 2.29 mA; 500 Ω

2.6 Power Considerations

Power rating is an important consideration in selecting resistors. The resistors must be capable of withstanding the maximum anticipated power without overheating. Power considerations also affect transistor selection. Designers normally select components that have the lowest power-handling capability suitable for the design. Frequently, *derating* is used to improve the reliability of a device. This is similar to using safety factors in the design of mechanical systems where the system is designed to withstand values that exceed the maximum.

2.6.1 *Derivation of Power Equations*

Average power is calculated as follows:

$$\text{for dc:} \quad P = VI = I^2R = \frac{V^2}{R}$$

$$\text{for ac:} \quad P = \frac{1}{T}\int_0^T v(t)i(t)dt$$

In the ac equation, T is one period of the waveform. If the signal is not periodic, we let T approach infinity. The power supplied by the power source to the CE amplifier of Figure 2.16 can be written as follows:

$$\begin{aligned} P_{V_{CC}} &= P_{(\text{transistor circuit})} + P_{(\text{bias current})} \\ &= \frac{1}{T}\int_0^T V_{CC}\,[I_{CQ} + i_c(t)]\,dt + \frac{V^2_{CC}}{R_1 + R_2} + I^2_{BQ}R_2 \\ &= V_{CC}I_{CQ} + \frac{V^2_{CC}}{R_1 + R_2} + I^2_{BQ}R_2 \end{aligned}$$

We have assumed that the average value of $i_c(t)$ is zero. For example, if the input ac signal is a sinusoid,

$$i_c(t) = A \sin \omega t$$

Then

$$\int_0^T A \sin \omega t \, dt = 0$$

where $T = 2\pi/\omega$. Since $I^2_{BQ}R_2$ is small, it usually can be ignored.

The average power dissipated by the transistor is

$$P_{(\text{transistor})} = \frac{1}{T}\int_0^T v_{CE}(t) i_C(t) \, dt \tag{2.20}$$

For zero-signal input, this becomes

$$P_{(\text{transistor})} = V_{CEQ} I_{CQ}$$

For an input signal with maximum possible swing,

$$\begin{aligned} v_{CE}(t) &= V_{CEQ} - V_{CEQ} \sin \omega t = V_{CEQ}(1 - \sin \omega t) \\ i_C(t) &= I_{CQ} + I_{CQ} \sin \omega t = I_{CQ}(1 + \sin \omega t) \\ P_{(\text{transistor})} &= \frac{1}{T}\int_0^T V_{CEQ} I_{CQ} (1 - \sin \omega t)(1 + \sin \omega t) \, dt \\ &= \frac{V_{CEQ} I_{CQ}}{T}\int_0^T (1 - \sin^2 \omega t) \, dt \\ &= \frac{V_{CEQ} I_{CQ}}{T}\int_0^T \cos^2 \omega t \, dt \\ &= \frac{V_{CEQ} I_{CQ}}{2T}\int_0^T (1 + \cos 2\omega t) \, dt \\ &= \frac{V_{CEQ} I_{CQ}}{2} \end{aligned} \tag{2.21}$$

From the above derivation, we see that the transistor dissipates its maximum power when no ac signal input is applied. This is shown in Figure 2.18. Depending upon the amplitude of the input signal, the transistor will dissipate an average power between $V_{CEQ}I_{CQ}$ and one-half of this value. Therefore, the transistor is selected for zero input signal so it will handle the maximum power as follows:

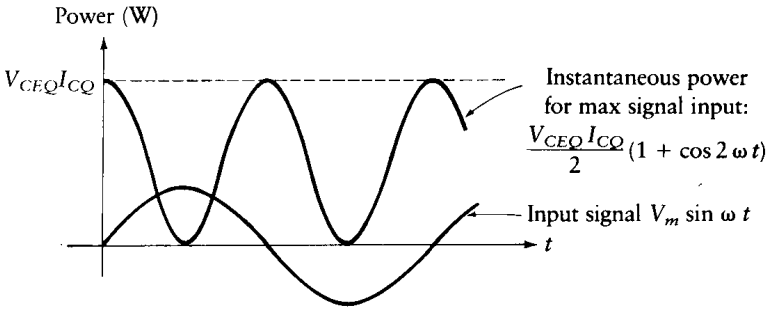


Figure 2.18
Instantaneous transistor power.

$$P_{(\text{transistor-max average})} = V_{CEQ}\, I_{CQ} \tag{2.22}$$

We need a measure of efficiency to determine how much of the power delivered by the source appears as signal power at the output. We define *conversion efficiency* as

$$\eta = \frac{P_o\ (\text{ac})}{P_{V_{CC}}\ (\text{dc})} \times 100$$

Drill Problems

D2.6 What is the maximum power used from the power supply in Problem D2.1?

Ans: 69.2 mW

D2.7 What would the maximum undistorted ac power in R_C be in Problem D2.1 when an ac signal is injected into the amplifier to obtain a maximum symmetrical output swing?

Ans: 2.94 mW

D2.8 What is the actual conversion efficiency of the amplifier in Problem D2.3?

Ans: 21%

2.7 Bypass and Coupling Capacitors

Capacitors are approximated as short circuits for ac signals and open circuits for dc signals. *Bypass capacitors* are therefore used to effectively eliminate

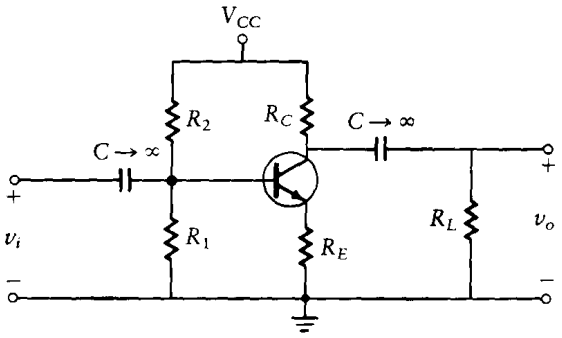


Figure 2.19
Common emitter ac amplifier stage.

(short out) resistors during ac operation. *Coupling capacitors* are used to block the direct current yet allow the ac signal to pass.

2.7.1 *Bypass Capacitors*

Capacitors can be used to bypass the emitter resistor, thus increasing the voltage gain of an amplifier. To accomplish this, a capacitor is selected so that its impedance at operating frequencies is much less than the resistance of the emitter resistor. Since impedance increases with decreasing frequency, the capacitor impedance should be much less than the value of the equivalent resistance across the capacitance at the lowest operating frequency of the amplifier.

2.7.2 *Coupling Capacitors*

Each pair of stages of a multistage amplifier can be coupled together with a capacitor. The input impedance of the following stage is the load of the previous stage. A coupling capacitor is necessary to prevent interactions of dc currents between adjacent stages. A single-stage transistor amplifier has the form shown in Figure 2.19, where R_L is the equivalent input resistance of the next stage.

The capacitors are open circuits at dc, and they are short circuits for ac (at the midfrequency operating region that we are addressing). However, the capacitors assume a major role in determining the low-frequency portion of the response curve. That role is addressed in Chapter 10.

2.8 ac Load Line for CE Configuration

Before beginning discussion of load lines for the CE amplifier, we note that the bias methods for CE and CB configurations are identical. Thus, although

we are presenting the theory for the CE, we use the same concepts for both CE and CB.

The resistance in the emitter-collector circuit for dc operation is $R_C + R_E$, which we define as R_{dc}. When a load is coupled to the transistor through a capacitor, the ac resistance is different. Under ac conditions, the resistance in the emitter-collector circuit is

$$R_{ac} = (R_L \parallel R_C) + R_E$$

Note that for ac operation, the V_{CC} terminal is grounded. If the emitter resistor is bypassed with a capacitor, then the ac resistance is only

$$R_{ac} = R_L \parallel R_C$$

The ac load line has a slope of $-1/R_{ac}$. Since a zero ac input places the operation at the Q-point, the ac load line intersects the dc load line at the Q-point. If the input signal is small, the Q-point should normally be located to minimize the quiescent collector current. In designing such circuits, we raise I_{CQ} above the zero point just enough to allow linear reproduction of the input signal (i.e., no distortion by entering the cutoff region). Under this condition, the transistor dissipates less power than if the Q-point is placed in the middle of the ac load line. We investigate this design procedure in Section 2.9.3.

2.8.1 *ac Load Line Through Any Q-Point*

We determined the dc load line from equation (2.12). This is then given by the equation

$$i_C = \frac{-v_{CE}}{R_E + R_C} + \frac{V_{CC}}{R_E + R_C}$$

Since the coupling capacitors are open circuits to dc, this load line applies to the circuit of Figure 2.19. The load line is plotted on the characteristic curves of Figure 2.20. The definitions of ac and dc resistance are repeated next.

R_{dc} = total resistance around the collector-emitter loop under dc conditions (capacitors considered open circuits)

R_{ac} = total resistance around the collector-emitter loop under ac conditions (dc sources set to zero and capacitors considered short circuits)

For the circuit in Figure 2.19, we have

$$R_{dc} = R_E + R_C \tag{2.23}$$

$$R_{ac} = R_L \parallel R_C + R_E \tag{2.24}$$

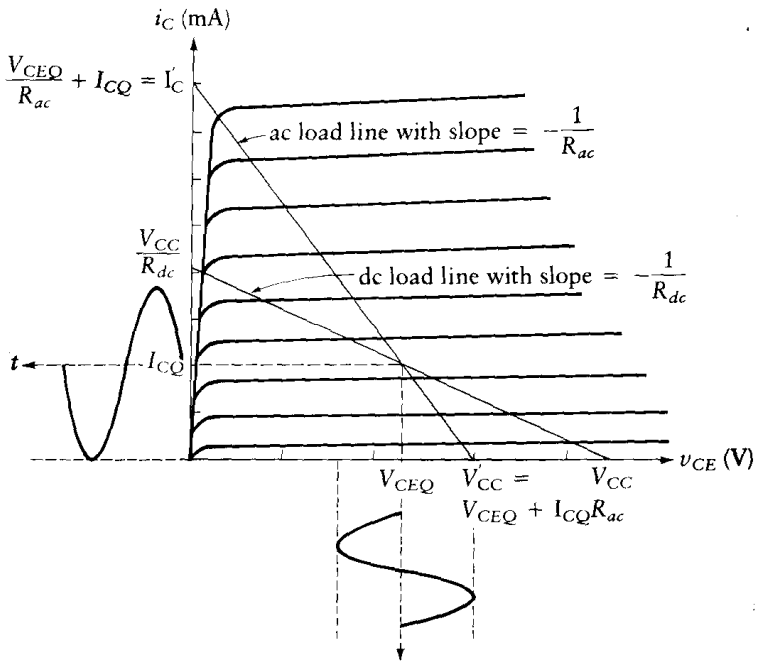


Figure 2.20
Characteristic curves.

The equation for the dc load line is then

$$i_C = \frac{V_{CC}}{R_{dc}} - \frac{v_{CE}}{R_{dc}} = \frac{1}{R_{dc}}(V_{CC} - v_{CE})$$

The Q-point, which is specified for zero signal value, is on both the ac and dc load lines. The ac load line goes through the Q-point and has a slope of $-1/R_{ac}$. This slope is greater in magnitude than that of the dc load line. The ac load line is plotted in Figure 2.20. The intersections with the i_C-axis and the v_{CE}-axis can be obtained from the equation for a straight line through a given point (x_1, y_1) with known slope (m) as follows:

$$(y - y_1) = m(x - x_1)$$

$$(i_C - I_{CQ}) = \frac{-(v_{CE} - V_{CEQ})}{R_{ac}}$$

$$i_C = -\frac{v_{CE}}{R_{ac}} + \left(\frac{V_{CEQ}}{R_{ac}} + I_{CQ}\right)$$

The intersection of the ac load line with the i_C-axis is then

$$I'_C = \frac{V_{CEQ}}{R_{ac}} + I_{CQ}$$

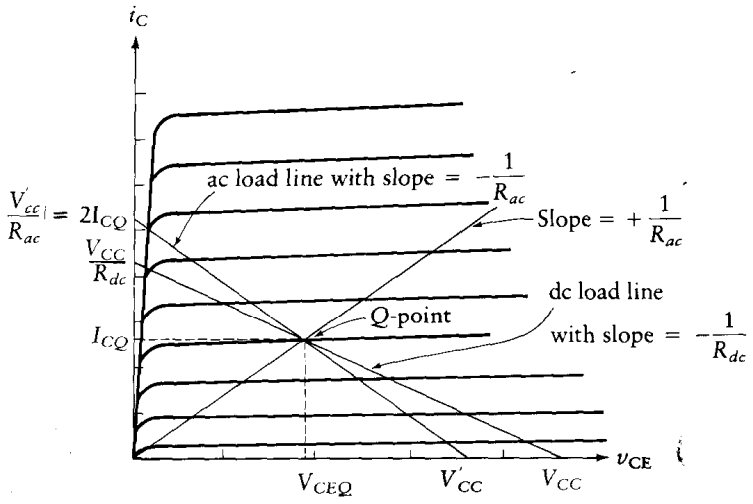


Figure 2.21
Load lines for maximum ac swing.

The intersection of the ac load line with the v_{CE}-axis is, with $i_C = 0$,

$$V'_{CC} = V_{CEQ} + I_{CQ}R_{ac}$$

2.8.2 *Choice of ac Load Line for Maximum Output Swing*

If we wish to design for the maximum output voltage swing from the amplifier, the Q-point must be placed in the center of the ac load line. Figure 2.21 shows the load lines for the circuit in Figure 2.19. It is a matter of geometry to set the Q-point for maximum swing. The dc load line is drawn as in Figure 2.20. That is,

$$V_{CC} = v_{CE} + i_C R_{dc} \tag{2.25}$$

We write KVL equations for the ac case, where capacitors are replaced by short circuits and the dc sources are set to zero. We write the linear equation with the point-slope method, as follows:

$$(i_C - I_{CQ}) = -\frac{1}{R_{ac}}(v_{CE} - V_{CEQ}) \tag{2.26}$$

The intersection of this line and the dc load line is the Q-point. Since i_C is maximum when $v_{CE} = 0$, the maximum collector current, I'_C, is given by

$$I'_C = \frac{V_{CEQ}}{R_{ac}} + I_{CQ}$$

However, I'_C is equal to $2I_{CQ}$ for maximum swing along the ac load line. Substituting this constraint in the previous equation, we obtain

$$2I_{CQ} - I_{CQ} = \frac{V_{CEQ}}{R_{ac}}$$

or

$$I_{CQ} = \frac{V_{CEQ}}{R_{ac}} \tag{2.27}$$

Equation (2.27) represents one equation in two unknowns for specifying the Q-point location for maximum output swing. The second equation is derived by using the dc load-line equation. Equation (2.27) is substituted into equation (2.25) as follows:

$$V_{CC} = V_{CEQ} + \frac{V_{CEQ}R_{dc}}{R_{ac}}$$

which reduces to

$$V_{CEQ} = \frac{V_{CC}}{1 + R_{dc}/R_{ac}} \tag{2.28}$$

This specifies v_{CE} at the Q-point. I_{CQ} is then found from equation (2.27) as follows:

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} \tag{2.29}$$

V'_{CC} is the intercept of the ac load line with the v_{CE}-axis, as shown in Figure 2.21. The slope of the ac load line is

$$\frac{-1}{R_{ac}} = \frac{-2I_{CQ}}{V'_{CC}}$$

so

$$V'_{CC} = 2I_{CQ}R_{ac} = \frac{2V_{CC}}{1 + R_{dc}/R_{ac}} \tag{2.30}$$

or

$$V'_{CC} = 2V_{CEQ}$$

2.9 ac Analysis and Design

We now have the necessary tools to permit analysis and design of amplifier circuits. It is necessary for us only to pull together the results derived in previous sections.

In *analyzing* an ac amplifier, the circuit components are specified. We begin the solution by determining the dc bias. The Thevenin equivalent circuit for the base-emitter loop is first derived. This provides the values needed to solve the bias equation for I_{CQ}. The dc and ac load lines are constructed next. If I_{CQ} is in the transistor operating region (i.e., not in the cutoff or saturation region), the maximum undistorted output ac voltage swing of the amplifier can be determined by examining the ac load line.

In *designing* an amplifier, the situation is reversed, since the designer must select the circuit components and has the option of selecting I_{CQ}. If a maximum output voltage swing is desired, I_{CQ} is placed in the center of the ac load line. On the other hand, if the input signal is small, I_{CQ} can be made just large enough so the ac signal output will not be clipped during the input signal maximum. In designing, the engineer starts calculations at the collector-emitter side of the amplifier rather than at the base-emitter side. After I_{CQ} has been determined, the bias equation is used to determine the values of R_1 and R_2 to cause the transistor to operate at the selected I_{CQ}.

2.9.1 *Analysis Procedure*

In analysis problems, the values of R_1, R_2, V_{CC}, V_{BE}, R_E, R_C, R_L, and β are given. We present an organized procedure for analysis. The equations used have been derived earlier in this chapter, and we cite references so the derivations can be consulted. We strongly recommend that you consult these derivations since it is important to be aware of the various assumptions. Our purposes in presenting this analysis procedure are not confined to teaching you the art of amplifier analysis. It is more important for you to appreciate the methodology of reducing theory to a step-by-step procedure. In this manner, you will be able to deal with new situations as they arise.

Step 1 Use R_1 and R_2 to determine V_{BB} and R_B from the following equations:

$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2}$$

$$R_B = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

(*Reference* equations (2.14) and (2.15))

Step 2 Use the bias equation to calculate I_{CQ}.

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E}$$

(*Reference* equation (2.13))

Step 3 The dc load line equation is used to determine V_{CEQ}.

$$V_{CEQ} = V_{CC} - (R_E + R_C)I_{CQ} = V_{CC} - R_{dc}I_{CQ}$$

(*Reference* equation (2.12))

Step 4 The dc load line is constructed on the characteristic curves. Since we know that the ac load line intersects the dc load line at the Q-point, the ac load line is constructed from the equation

$$V'_{CC} = V_{CEQ} + I_{CQ}(R_{ac})$$

where R_{ac} is the ac equivalent resistance in the collector-emitter loop.

(*Reference* last equation in Section 2.8.1)

Step 5 Determining the maximum possible symmetrical output voltage swing requires the use of the load-line construction on the characteristic curves. If the Q-point is on the upper half of the ac load line, I_{CQ} is subtracted from the maximum value of i_C (the point where the ac load line intersects the i_C axis). This provides the maximum amplitude ac output current of the transistor. Alternatively, if the Q-point is on the lower half of the ac load line, I_{CQ} is the maximum amplitude ac output current of the transistor. Then, the maximum peak-to-peak symmetrical output voltage swing is given by

$$2i_C(\text{maximum amplitude}) \times (R_C \parallel R_L)$$

2.9.2 *Design Procedure*

In design problems, we work first with the collector-emitter side of the transistor rather than with the base side. There are two conditions to satisfy. The first condition places the Q-point in the center of the ac load line for maximum output voltage swing. The second condition limits I_{CQ} to the value required to provide symmetrical output for a designated intput. V_{CC}, V_{BE}, β, and R_L are usually specified. R_C and R_E are determined by the other specified conditions of voltage gain, current gain, and input resistance. This is considered in Chapter 3. For now, the values of R_C and R_E are given.

Step 1 To place the Q-point in the center of the load line, use the following equation.

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}}$$

(*Reference* equation (2.29))

Step 2 Use the ac load line equation to determine V_{CEQ}.

$$V_{CEQ} = \frac{V'_{CC}}{2}$$

where

$$V'_{CC} = 2I_{CQ}R_{ac}$$

(*Reference* equation (2.30))

Step 3 If no other restrictions exist, select R_B for bias stability.

$$R_B = 0.1\ \beta R_E$$

(*Reference* equation (2.18))

Step 4 Use the bias equation to determine V_{BB}.

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E\right)$$

(*Reference* equation (2.13))

Step 5 Find R_1 and R_2 from R_B and V_{BB}.

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}}$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}}$$

(*Reference* equations (2.16) and (2.17))

Step 6 Determine $v_{o(p-p)}$ (maximum peak-to-peak symmetrical output) as in Step 5 of the analysis procedure.

$$V_o = 2i_C \text{ (maximum amplitude)} \times (R_C \parallel R_L)$$

Example 2.3 Analysis

Determine the Q-point for the circuit given in Figure 2.22 if $R_1 = 1.5\ \text{k}\Omega$ and $R_2 = 6\ \text{k}\Omega$. A 2N3903 transistor (see Appendix D) is used with $\beta = 140$, $R_E = 100\ \Omega$, and $R_C = R_L = 1\ \text{k}\Omega$.

SOLUTION Using the step-by-step procedure of this section, we obtain

$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2} = \frac{1500 \times 5}{1500 + 6000} = 1\ \text{V}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = 1200\ \Omega$$

We determine if the amplifier maintains bias stability with changes in β by checking $R_B < 0.1\beta R_E = 0.1(140)(100) = 1400\ \Omega$. Since the inequality holds, bias stability is maintained. We find the Q-point as follows:

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} = \frac{1 - 0.7}{1200/140 + 100} = 2.76\ \text{mA}$$

We find $R_{ac} = R_C \parallel R_L = 500\ \Omega$ and $R_{dc} = R_C + R_E = 1.1\ \text{k}\Omega$.

V_{CEQ} is found as in Step 3.

$$V_{CEQ} = V_{CC} - I_{CQ}R_{dc} = 5 - (2.76 \times 10^{-3})(1.1 \times 10^{3}) = 1.96\ \text{V}$$

Then

$$V'_{CC} = V_{CEQ} + I_{CQ}R_{ac} = 1.96 + (2.76 \times 10^{-3})(500) = 3.34\ \text{V}$$

Since the Q-point is on the lower half of the ac load line, the maximum possible symmetrical output voltage swing is then

$$2I_{CQ}(R_C \parallel R_L) = 2(2.76 \times 10^{-3})(500) = 2.76\ \text{V}$$

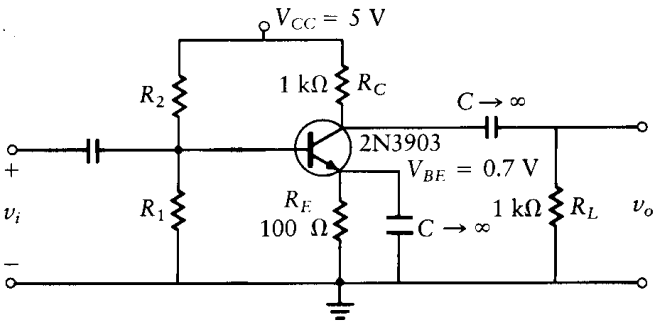


Figure 2.22
CE amplifier circuit.

The Q-point in this example is not in the middle of the load line, so that output swing is not a maximum. However, if the input signal is small and maximum output is not required, a small I_{CQ} can be used to reduce the power dissipated in the circuit.

Example 2.4 Design

Select R_1 and R_2 for maximum output voltage swing in the circuit shown in Figure 2.22.

SOLUTION Following the design steps of Section 2.9.2, we first determine I_{CQ} for the circuit:

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{5}{500 + 1100} = 3.13 \text{ mA}$$

since

$$R_{ac} = R_C \parallel R_L = 500\ \Omega$$

and

$$R_{dc} = R_E + R_C = 1100\ \Omega$$

For maximum swing,

$$V'_{CC} = 2V_{CEQ}$$

V_{CEQ} is then given by

$$V_{CEQ} = (3.13 \text{ mA})(500\ \Omega) = 1.56 \text{ V}$$

The intersection of the ac load line on the v_{CE}-axis is V'_{CC}. Since

$$V_{CEQ} = \frac{V'_{CC}}{2}$$

then

$$V'_{CC} = 3.12 \text{ V}$$

From the manufacturer's specification in Appendix D, **β for the 2N3903 is** approximately 140. R_B is set equal to 0.1 βR_E, so

$$R_B = 0.1(140)(100) = 1400\ \Omega$$

$$V_{BB} = (3.13 \times 10^{-3})\frac{1400}{140} + 100 + 0.7 = \mathbf{1.044\ V}$$

Since we know V_{BB} and R_B, we find R_1 and R_2:

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{1400}{1 - 1.044/5} = \mathbf{1.77\ k\Omega}$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{1400 \times 5}{1.044} = 6.7\ \text{k}\Omega$$

The maximum output voltage swing, ignoring the nonlinearities at saturation and cutoff, would then be

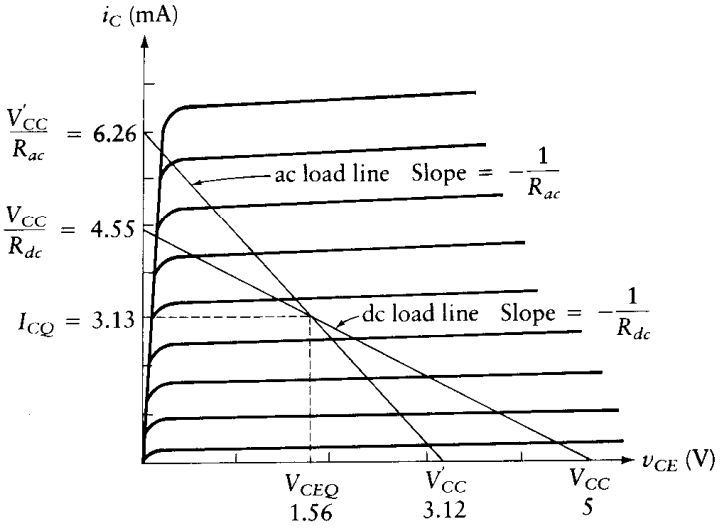
$$\text{maximum output swing} = 2I_{CQ}\,(R_C \parallel R_L)$$
$$= 2(3.13\ \text{mA})(500\ \Omega) = 3.13\ \text{V}$$

The load lines are shown on the characteristic curves of Figure 2.23.

We check the maximum power dissipated by the transistor to assure that it will not exceed the specifications. From equation (2.22), we have

$$P_{(\text{transistor})} = (1.56\ \text{V})(3.13\ \text{mA}) = \mathbf{4.88\ mW}$$

Figure 2.23 Load lines for Example 2.4.



This is well within the 350 mW maximum given on the specification sheet. The maximum conversion efficiency is

$$\eta = \frac{P_o(\text{ac})}{P_{V_{CC}}(\text{dc})} \times 100 = \frac{(3.13 \times 10^{-3}/2)^2 1000/2 \times 100}{5 \times 3.13 \times 10^{-3} + 5^2/8470)} = 6.6\%$$

Drill Problems

D2.9 Refer to Figure 2.19 and find the peak-to-peak output voltage swing when $R_1 = 2$ kΩ, $R_2 = 15$ kΩ, $R_E = 200$ Ω, $R_C = 2$ kΩ, $R_L = 2$ kΩ, $\beta = 200$, $V_{BE} = 0.7$ V, and $V_{CC} = 15$ V.

Ans: 6.3 V peak-to-peak

D2.10 In Problem D2.9, design the amplifier for maximum symmetrical swing by finding the values of R_1 and R_2.

Ans: $R_1 = 4.5$ kΩ; $R_2 = 36$ kΩ

D2.11 What is the maximum symmetrical voltage swing for the configuration of Problem D2.10?

Ans. 8.8 V peak-to-peak

D2.12 What is the output power of the amplifier of Problem D2.10? What is the power supplied to the amplifier?

Ans: 4.9 mW; 71.7 mW

2.9.3 *Designing for Less than Maximum Swing*

As discussed earlier, it is not always desirable to design an amplifier for maximum possible swing. If the input signal is small, the operating point may move only a relatively small distance on either side of the Q-point and never get near saturation or cutoff. In that case, designing an amplifier with the Q-point in the middle of the load line wastes power. The power dissipated in the rest condition is greater than necessary for undistorted operation. In this section, we modify the previous design criteria to allow for placement of the Q-point below the center of the load line.

Suppose we wish to design for a quiescent current,

$$I_{CQ} = \delta I'_C \tag{2.31}$$

where I'_C is the intersection of the ac load line with the i_C axis and is seen to be (Figure 2.20)

$$I'_C = \frac{V'_{CC}}{R_{ac}} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \tag{2.32}$$

Here δ is a number between 0 and 1 and is equal to 0.5 for the maximum symmetrical swing case. Now since

$$I_{CQ} = \delta I'_C$$

we can solve equation (2.32) for V_{CEQ} to obtain

$$V_{CEQ} = \frac{(1 - \delta)I_{CQ}R_{ac}}{\delta} \tag{2.33}$$

Since the Q-point must also lie on the dc load line, we have

$$V_{CEQ} = V_{CC} - I_{CQ}R_{dc} \tag{2.34}$$

Equating equation (2.33) to equation (2.34) yields

$$\frac{(1 - \delta)I_{CQ}R_{ac}}{\delta} = V_{CC} - I_{CQ}R_{dc}$$

and solving for I_{CQ}, we obtain

$$I_{CQ} = \frac{V_{CC}}{(1 - \delta)R_{ac}/\delta + R_{dc}} \tag{2.35}$$

Note that if $\delta = 0.5$, equation (2.35) reduces to

$$I_{CQ} = \frac{V_{CC}}{(R_{ac} + R_{dc})}$$

as found earlier.

2.10 Emitter-Follower (Common-Collector) Amplifier

The *emitter-follower (EF)*, or common-collector (CC), amplifier is illustrated in Figure 2.24. Its output is developed from the emitter to ground rather than from the collector to ground, as in the case of the CE. This type of amplifier configuration is used to obtain *current gain* and *power gain*.

The CE has a 180° phase shift between the base and collector voltages.

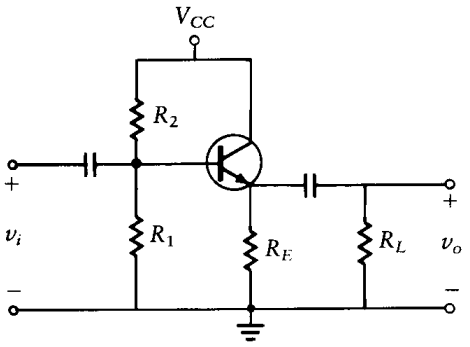


Figure 2.24
Emitter follower.

NOTE: Throughout this text, when a capacitor in a circuit is unlabelled, assume its capacitance approaches infinity (i.e. it is a short circuit for all signal frequencies).

That is, as the input signal increases in value, the output signal decreases. Alternatively, for an EF, the output signal is in phase with the input signal. The amplifier has a voltage gain of slightly less than unity. On the other hand, the current gain is significantly greater than 1. Note that the collector needs no resistor ($R_C = 0$), and no emitter bypass capacitor is required.

We analyze this circuit in the same manner as we did for the common emitter. The only differences are the values we use for R_{ac} and R_{dc}. For the emitter follower of Figure 2.24,

$$R_{ac} = R_E \parallel R_L$$

and

$$R_{dc} = R_E$$

and the dc load line is given by the equation

$$i_C = \frac{(V_{CC} - v_{CE})}{R_{dc}}$$

The ac load line, under conditions of maximum swing, is found in the same manner as for the common emitter circuit. For maximum swing, the Q-point is located at

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{V_{CC}}{(R_E \parallel R_L) + R_E}$$

and

$$V_{CEQ} = I_{CQ}R_{ac} = I_{CQ}(R_E \parallel R_L)$$

2.10.1 *ac Analysis and Design of EF Amplifiers*

The procedures for both design and analysis of EF amplifier are the same as those for CE amplifiers. The only changes are in the equations for R_{ac}, R_{dc}, and the output voltage swing. The output swing for the EF is given by

$$V_{om} = 2i_C(\text{max amplitude}) \times (R_E \parallel R_L) \tag{2.36}$$

Example 2.5 Design

In the circuit of Figure 2.25(a), find the values of R_1 and R_2 that yield maximum symmetrical output swing as shown in Figure 2.25(b). Assume that a 2N2222 transistor is used (see Appendix D for data sheets) with an average β of 100.

SOLUTION

$$R_{dc} = R_E = 600\ \Omega$$

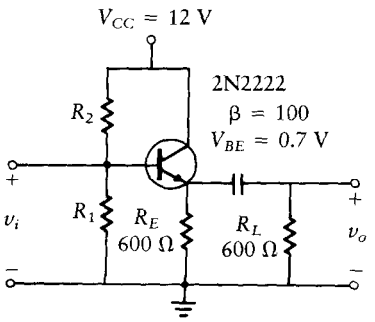
$$R_{ac} = R_E \parallel R_L = 300\ \Omega$$

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{12}{600 + 300} = 13.3\ \text{mA}$$

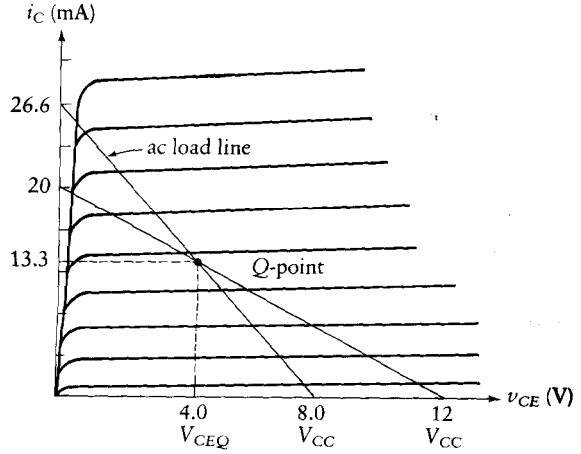
Then

$$V_{CEQ} = I_{CQ}R_{ac} = (13.3 \times 10^{-3})(300) = 4\ \text{V}$$

Figure 2.25 EF amplifier for Example 2.5.



(a)



(b)

In order to reduce the effects of variations in β, we choose

$$R_B = 0.1\,\beta R_E = 0.1(100 \times 600) = 6\ \text{k}\Omega$$

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E\right)$$

$$= 0.7 + 0.0133\left(\frac{6000}{1000} + 600\right) = \mathbf{9.48\ V}$$

From equations (2.16) and (2.17) we obtain

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{6000}{1 - 9.48/12} = 28.5\ \text{k}\Omega$$

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{6000 \times 12}{9.48} = 7.59\ \text{k}\Omega$$

From equation (2.36), we find

$$\text{maximum output swing} = 2I_{CQ}(R_E \parallel R_L)$$

$$= 2(0.0133)(300) = 7.98\ \text{V}$$

Example 2.6 Analysis

Find the Q-point and output voltage swing of the circuit of Figure 2.25(a) with $R_1 = 10\ \text{k}\Omega$ and $R_2 = 20\ \text{k}\Omega$.

SOLUTION Using equation (2.14) and equation (2.15), we have

$$R_B = R_1 \parallel R_2 = 6.67\ \text{k}\Omega$$

$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2} = \frac{12(10 \times 10^3)}{30 \times 10^3} = \mathbf{4\ V}$$

From equation (2.13), we have

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} = \frac{4 - 0.7}{6670/100 + 600} = 4.9\ \text{mA}$$

The output swing is then given by

$$\text{output swing} = 2I_{CQ}(R_E \parallel R_L)$$

$$= 2(4.95 \times 10^{-3})(300) = 2.98\ \text{V}$$

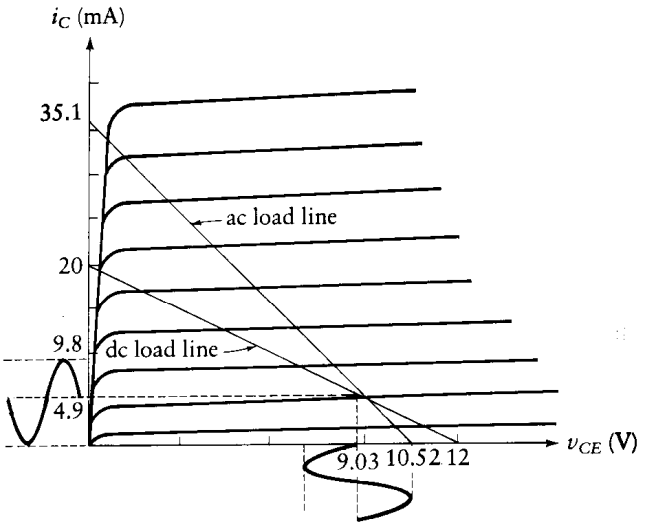


Figure 2.26
Load lines for Example 2.6.

This is less than the maximum possible output swing. Continuing the analysis,

$$V_{CEQ} = V_{CC} - I_{CQ}R_E$$
$$= 12 - (4.95 \times 10^{-3})(600) = 9.03 \text{ V}$$
$$V'_{CC} = V_{CEQ} + I_{CQ}(R_E \parallel R_L)$$
$$= 9.03 + (4.95 \times 10^{-3})(300) = 10.52 \text{ V}$$
$$I'_C = \frac{10.52}{300} = 35.1 \text{ mA}$$

The load lines for this problem are shown in Figure 2.26

Drill Problems

D2.13 What is the maximum symmetrical voltage swing for the amplifier of Figure 2.24, where $V_{CC} = 15$ V, $R_1 = 8$ kΩ, $R_2 = 2$ kΩ, $R_E = 1$ kΩ, $R_L = 1$ kΩ, $V_{BE} = 0.7$ V, and $\beta = 80$?

Ans: 7.8 V peak-to-peak

D2.14 In Problem D2.13, redesign the amplifier for the maximum symmetrical voltage swing. What are the new values of R_1, R_2, and $V_{o(p-p)}$?

Ans: 36.4 kΩ; 10.3 kΩ; 10 V peak-to-peak

D2.15 What is the conversion efficiency of the amplifier design in Problem D2.14?

Ans: 8%