

TECHNICAL UNIVERSITY OF KOŠICE
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DEPARTMENT OF ELECTRONICS AND MULTIMEDIA
COMMUNICATIONS

BASIC OF ELECTRONICS

Lecture 11

2008/09

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Applied Informatics

Contents

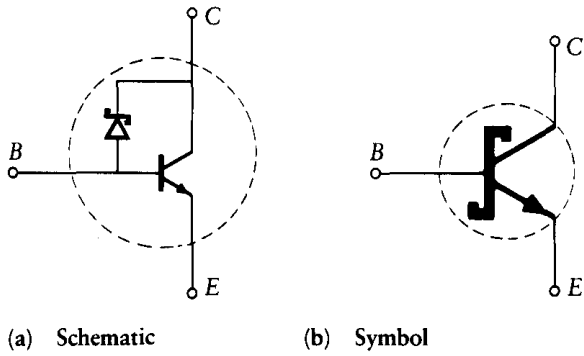
Lecture 11:

Difference Amplifiers

Current Sources, Active Loads and Level Shifters

References and Sources

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(a) Schematic (b) Symbol

Figure 7.2 Schottky npn transistor.

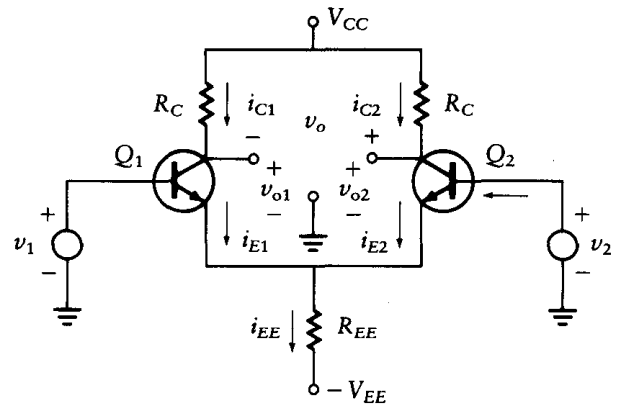


Figure 7.3 Differential amplifier.

7.2 Difference Amplifiers

Most operational amplifiers are comprised of a series of transistors, resistors, and capacitors, which form a complete system on a single chip. The amplifiers available today are highly reliable, small in size, and consume a small amount of power.

The input stage of most op-amps is a *difference amplifier*, as shown in its simplest form in Figure 7.3. The *difference amplifier* (or differential amplifier) is composed of two emitter-coupled CE dc amplifiers with two inputs, v_1 and v_2 , and three outputs, v_{o1} , v_{o2} , and v_o . The third output, v_o , is the difference between v_{o1} and v_{o2} . This can be verified by applying the superposition principle to the circuit.

7.2.1 dc Transfer Characteristics

The difference amplifier does not operate linearly with large signal inputs. In order to simplify the analysis, we assume that R_E is large, that the base resistance of the transistors is negligible, and that the output resistance of the transistors is large. The large R_E keeps the emitter resistor voltage drop constant.

We begin by writing a KVL equation around the base junction loop for the circuit of Figure 7.3 under ac conditions:

$$v_1 = v_{BE1} - v_{BE2} + v_2 \tag{7.1}$$

We solve the circuit for the collector currents, i_{C1} and i_{C2} . The base-emitter voltage is given by the equation presented in Section 3.2.

$$v_{BE1} = V_T \ln\left(\frac{i_{C1}}{\beta I_{o1}}\right) \quad (7.2)$$

$$v_{BE2} = V_T \ln\left(\frac{i_{C2}}{\beta I_{o2}}\right) \quad (7.3)$$

Since the transistors are assumed to be identical, we have

$$I_{o1} = I_{o2}$$

Combining equations (7.1), (7.2), and (7.3) yields

$$v_1 - V_T \ln\left(\frac{i_{C1}}{\beta I_{o1}}\right) + V_T \ln\left(\frac{i_{C2}}{\beta I_{o2}}\right) - v_2 = 0$$

and

$$\frac{i_{C1}}{i_{C2}} = \exp\left[\frac{v_1 - v_2}{V_T}\right] \quad (7.4)$$

We assume that i_C is approximately equal to i_E . Therefore,

$$i_{EE} = i_{C1} + i_{C2} \quad (7.5)$$

Combining equation (7.4) and equation (7.5), we have

$$i_{C1} = \frac{i_{EE}}{1 + \exp[-(v_1 - v_2)/V_T]} \quad (7.6)$$

$$i_{C2} = \frac{i_{EE}}{1 + \exp[(v_1 - v_2)/V_T]} \quad (7.7)$$

Note that

$$v_o = (i_{C1} - i_{C2})R_C$$

An important observation can be made by viewing equations (7.6) and (7.7). If $v_1 - v_2$ becomes greater than several hundred millivolts, the collector current in transistor 2 becomes extremely small and the transistor is essentially cut off. The collector current in transistor 1 is approximately equal to i_{EE} , and this transistor is saturated. The collector currents, and therefore the output voltage v_o , become independent of the difference between the two input voltages. Linear amplification occurs only for input voltage differences less than approximately 100 mV.

In order to increase the linear range of the input voltage, small emitter resistors can be added. This causes a negative feedback condition, resulting in the reduction in the voltage amplification.

7.2.2 Common-Mode and Differential-Mode Gains

The difference amplifier is intended to respond only to the difference between the two input voltages, v_1 and v_2 . However, in a practical op-amp, the output depends to some degree upon the sum of these inputs. Thus, for example, if both inputs are equal, the output voltage should be zero, but in a practical amplifier it is not. We label the case when the circuit responds to the difference as the *differential-mode* case. If the two inputs are made equal, we say the circuit is in its *common mode*. Ideally we would expect the circuit to produce an output only in the differential mode.

Any two input voltages can be resolved into a common and a differential part. That is, we define two new input voltages as follows:

$$\begin{aligned} v_{di} &= v_1 - v_2 \\ v_{ci} &= \frac{v_1 + v_2}{2} \end{aligned} \quad (7.8)$$

The voltage v_{di} is the differential-mode input voltage and it is simply the difference between the two input voltages. The voltage v_{ci} is the common-mode input voltage, and it is the average of the two input voltages. The original input voltages can be expressed in terms of these new quantities as follows:

$$\begin{aligned} v_1 &= \frac{v_{di} + 2v_{ci}}{2} \\ v_2 &= \frac{2v_{ci} - v_{di}}{2} \end{aligned} \quad (7.9)$$

If we set the two input voltages equal, we have

$$v_1 = v_2 = v_{ci}$$

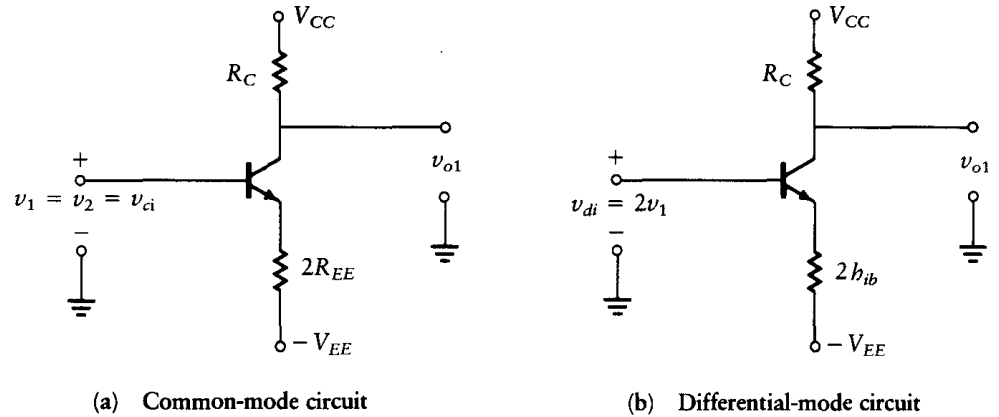
and

$$v_{di} = 0$$

f.

Since the two inputs are equal and the transistors are identical, the emitter-base junction voltages will be equal. Thus, the collector currents must also be identical. Since the emitter currents will be equal, we analyze a half-circuit as shown in Figure 7.4(a). Note that the emitter resistance has been doubled, since

Figure 7.4
Differential-amplifier
analysis.



the actual current in this resistor is twice that maintained by the illustrated half-circuit. The output of the half-circuit is v_{o1} or v_{o2} . We define a common-mode and differential-mode gain by resolving the output into two components,

$$v_{o1} = A_d v_{di} + A_c v_{ci}$$

The common-mode gain is found by setting the two inputs equal, since we have forced v_{di} to be zero. Thus, assuming the r_o of the BJT is large and $h_{ib} \ll R_{EE}$, then

$$A_c = \frac{v_{o1}}{v_{ci}} = \frac{-R_C}{2R_{EE}} \quad (7.10a)$$

In order to find the differential-mode gain, we again use the technique of splitting the circuit in two parts and analyze the half-circuit of Figure 7.4(b). We let

$$v_1 = -v_2$$

so

$$v_{di} = 2v_1 = -2v_2$$

The ac current from one emitter flows directly into the other emitter, so the voltage across the emitter resistor remains constant. Since the ac signal voltage across the resistor is zero, it can therefore be replaced by a short circuit in the ac equivalent circuit. However, the resistance, h_{ib} , remains in the base-emitter loop of the transistor. The differential-mode gain is then given by

$$A_d = \frac{v_{o1}}{v_{di}} = \frac{-R_C}{2h_{ib}} \quad (7.10b)$$

Note that the common-mode gain is defined in terms of only one of the two outputs. The differential output, v_o , should (ideally) cancel to zero. In the practical circuit, parameter variations occur. If the common-mode gain is high, these variations affect v_o as well as the two individual output voltages. For this reason, it is desirable for the differential-mode gain to be much larger than the common-mode gain. The *common-mode rejection ratio* (CMRR) is defined as the ratio of the differential-mode gain to the common-mode gain (usually expressed in decibels).

$$\text{CMRR} = 20 \log \frac{|-R_C/2h_{ib}|}{|-R_C/2R_{EE}|} \text{ dB} = 20 \log \left(\frac{R_{EE}}{h_{ib}} \right) \text{ dB} \quad (7.11)$$

It is desirable to make the CMRR as large as possible so that the amplifier will react only to the difference between the input voltages.

Before we evaluate the differential-mode and common-mode gain, let us look at the input resistance of the amplifier in both the differential mode and the common mode. For the differential mode, we look into the amplifier at the base of both transistors. This results in a complete circuit through the emitter of both transistors, and the input resistance is

$$R_i(\text{differential mode}) = 2h_{ie}$$

Now from the common-mode input, we look into the amplifier in Figure 7.4(a). Thus, the input resistance is

$$R_i(\text{common mode}) = 2\beta R_{EE}$$

These results indicate that the input resistance of the common mode is much higher than that of the differential mode.

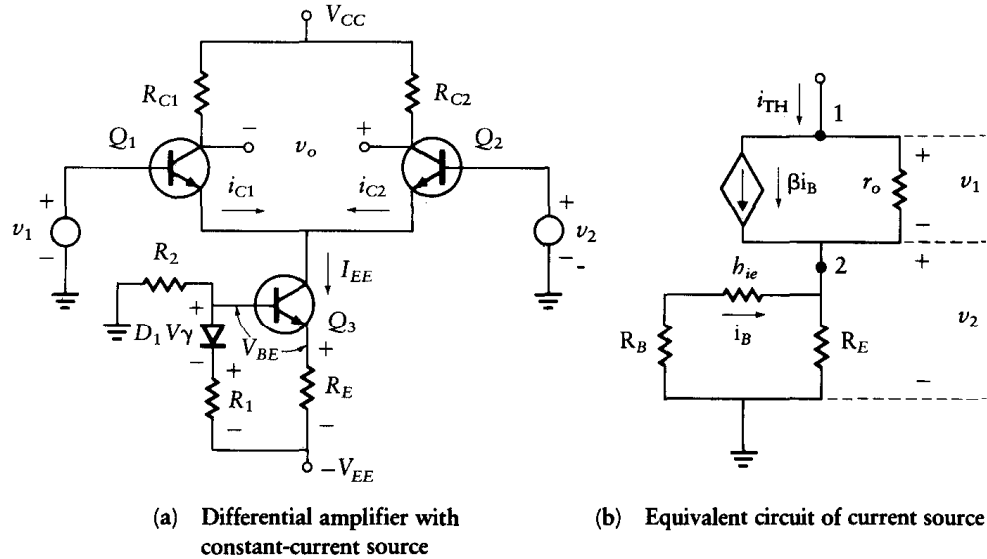
Equation (7.11) shows that to make the CMRR large, we must make R_{EE} large. Since large resistances are hard to fabricate on IC chips, we seek an alternate approach. This is accomplished by replacing R_{EE} with a constant-current generator, as we discuss in the next section.

Our differential-amplifier analysis is based upon BJTs as the transistor building blocks. Junction field-effect transistors can also be used in differential amplifiers, with the resulting advantages of reduced input bias current and higher input impedance. However, the analysis of the differential amplifier using JFETs is accomplished in the same way as that of BJT analysis.

7.2.3 Differential Amplifier with Constant-Current Source

In the previous section, we saw that it is desirable to make R_{EE} as large as possible in order to reduce the common-mode output. An ideal constant-current source has infinite impedance, so we investigate the possibility of replacing

Figure 7.5
Differential amplifier
with constant-current
source.



R_{EE} with such a current source. Figure 7.5 illustrates a differential amplifier where the resistor, R_{EE} , is replaced with a constant-current source.

The closer the source is to the ideal constant current source, the higher the CMRR. We therefore show a diode-compensated current source. The compensation, as discussed in Section 5.4, makes the operation of the circuit less dependent upon temperature variations. Diode D_1 and transistor Q_3 are selected so that they have nearly identical characteristics over the range of operating temperatures.

In order to analyze the circuit of Figure 7.5(a) and find the CMRR, we need to determine the equivalent resistance, R_{TH} , the Thevenin equivalent of the constant current source circuit. Looking at the equivalent circuit of the current source as shown in Figure 7.5(b), we have

$$R_{TH} = \frac{v_1 + v_2}{i_{TH}}$$

Writing a KCL equation at node 1, we have

$$i_{TH} = \beta i_B + \frac{v_1}{r_o}$$

where r_o is the internal resistance of the transistor at the specified operating point (see Section 3.1.2).

A KCL equation at node 2 yields

$$\beta i_B + \frac{v_1}{r_o} + i_B - \frac{v_2}{R_E} = 0$$

but

$$v_1 = (i_{TH} - \beta i_B)r_o$$

and

$$v_2 = -i_B(h_{ie} + R_B)$$

Substituting v_1 and v_2 into the equation at node 2, we have

$$-i_{TH} = i_B + \frac{h_{ie} + R_B}{R_E} i_B = i_B \left(1 + \frac{h_{ie} + R_B}{R_E} \right)$$

The Thevenin resistance is given by

$$R_{TH} = \frac{h_{ie} + R_B + r_o[1 + (h_{ie} + R_B)/R_E] + \beta r_o}{1 + (h_{ie} + R_B)/R_E}$$

In order to maintain bias stability, we have used the guideline that

$$R_B = 0.1\beta R_E$$

Substituting this value of R_B in the equation for R_{TH} and dividing by β , we have

$$R_{TH} = \frac{h_{ib} + 0.1R_E + r_o [1/\beta + (h_{ib} + 0.1R_E)/R_E + 1]}{1/\beta + (h_{ib} + 0.1R_E)/R_E}$$

Since

$$1 \gg \frac{1}{\beta}$$

and

$$\frac{h_{ib} + 0.1R_E}{R_E} \gg \frac{1}{\beta}$$

we have

$$R_{TH} = \frac{h_{ib} + 0.1R_E + r_o [1 + (h_{ib} + 0.1R_E)/R_E]}{(h_{ib} + 0.1R_E)/R_E}$$

and

$$R_{TH} = R_E + r_o \left[1 + \frac{R_E}{h_{ib} + 0.1R_E} \right]$$

Since the second term in this equation is much greater than the first, we can ignore R_E to get

$$R_{TH} = r_o \left[1 + \frac{R_E}{h_{ib} + 0.1R_E} \right]$$

This equation can be further simplified if the following condition exists:

$$0.1R_E \gg h_{ib}$$

In that case, we have the simple result

$$R_{TH} \approx 11r_o \quad (7.12)$$

Hence, if all of the approximations are valid, R_{TH} is independent of β and its value is quite large.

7.2.4 Differential Amplifier with Single-Ended Input and Output

Figure 7.6 shows a differential amplifier where the second input, v_2 , is set equal to zero and the output is taken as v_{o1} .

We use a constant-current source in place of R_E , as discussed in the previous section. This is known as a *single-ended input and output amplifier with phase reversal*. The amplifier is analyzed by setting $v_2 = 0$ in the earlier equations. The differential input is then simply

$$v_{di} = v_1 - v_2 = v_i$$

so the output is

$$v_o = v_{o1} = A_d v_{di} = \frac{-R_C v_i}{2h_{ib}}$$

The minus sign indicates that this amplifier exhibits a 180° phase shift between the output and input. A typical sinusoidal input and output are illustrated in the figure.

If an output signal is to be referenced to ground but a phase reversal is not desired, the output can be taken from transistor Q_2 , as illustrated in Figure

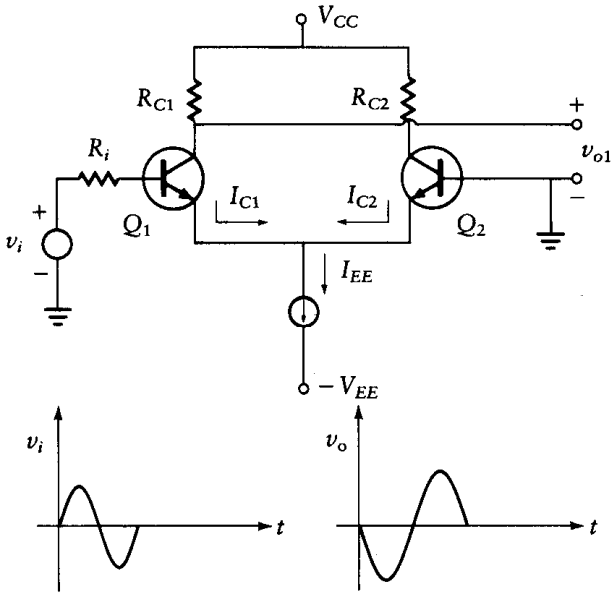


Figure 7.6 Single-ended input with phase reversal.

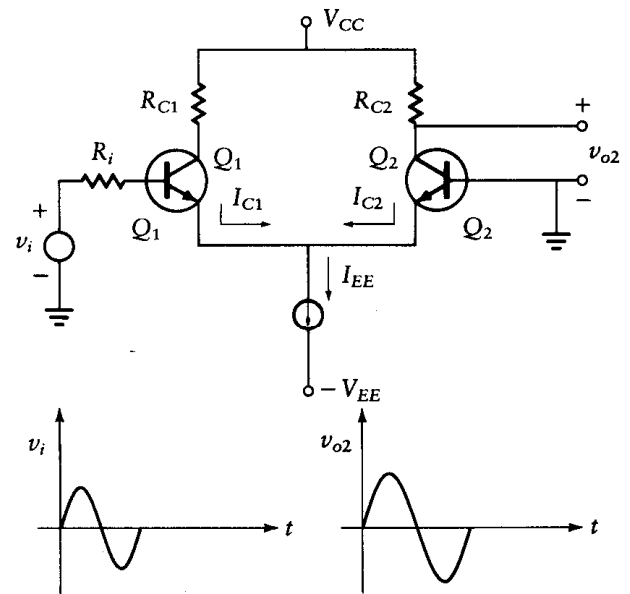


Figure 7.7 Single-ended input with in-phase output.

7.7. In order to show that the output of the circuit of Figure 7.7 is the inverse of that of Figure 7.6, take the mirror image of the first circuit. That is, suppose $v_1 = 0$ and $v_2 = v_i$ in the original differential amplifier of Figure 7.3. The differential-input voltage is then

$$v_{di} = v_1 - v_2 = -v_i$$

Thus, the output is the negative of that found earlier, and no phase reversal occurs.

Example 7.1 Differential Amplifier (Analysis)



Find the differential voltage gain, the common-mode voltage gain, and the CMRR for the circuit shown in Figure 7.3. Assume that $R_i = 0$, $R_C = 5 \text{ k}\Omega$, $V_{EE} = 15 \text{ V}$, $V_{BE} = 0.7 \text{ V}$, $V_T = 26 \text{ mV}$, and $R_{EE} = 25 \text{ k}\Omega$. Let $v_2 = 0$ and take output from v_{o2} .

SOLUTION The current in the current source is found at the quiescent conditions. Since the base of Q_2 is grounded, the emitter voltage is $-V_{BE} = -0.7 \text{ V}$, and

$$I_{EE} = \frac{V_{EE} - V_{BE}}{R_{EE}} = \frac{15 - 0.7}{25,000} = 0.57 \text{ mA}$$

The quiescent current in each transistor is one-half of this amount

$$I_{C1} = I_{C2} = \frac{I_{EE}}{2} = 0.29 \text{ mA}$$

Since

$$h_{ib} = \frac{V_T}{I_C} = \frac{26}{0.29} = 90 \Omega$$

the differential voltage gain in each transistor is

$$A_d = \frac{-R_C}{2h_{ib}} = \frac{5000}{2(90)} = -28$$

The common-mode voltage gain is

$$A_c = \frac{-R_C}{2R_{EE}} = \frac{-5000}{50,000} = -0.1$$

The common-mode rejection ratio is then given by

$$\text{CMRR} = 20 \log \left(\frac{|A_d|}{|A_c|} \right) = 49 \text{ dB}$$



Example 7.2



For the differential amplifier described in Example 7.1, design a current source to replace R_{EE} and determine the new CMRR for the differential amplifier, with $r_o = 105 \text{ k}\Omega$, $V_{BE} = 0.7 \text{ V}$, and $\beta = 100$.

SOLUTION We place the transistor operating point in the middle of the dc load line.

$$V_{CEQ} = \frac{V_{EE} - V_{BE}}{2} = \frac{15 - 0.7}{2} = 7.15 \text{ V}$$

Then, referring to the current source of Figure 7.5a,

$$R_{EE} = \frac{7.15 \text{ V}}{0.57 \text{ mA}} = 12.54 \text{ k}\Omega$$

For bias stability,

$$R_B = 0.1 \beta R_{EE} = 0.1(100)(12,540) = 125.4 \text{ k}\Omega$$

Since $0.1R_E \gg h_{ib}$ (i.e., $1.25 \text{ k}\Omega \gg 90 \Omega$), then from equation (7.12), we have

$$R_{TH} \approx 11r_o$$

so the equivalent resistance and CMRR are given by

$$R_{TH} \approx 11 (105 \text{ k}\Omega) = 1.155 \text{ M}\Omega$$

$$\text{CMRR} = 20 \log \left(\frac{R_{TH}}{h_{ib}} \right) = 20 \log \left(\frac{1.155 \times 10^6}{90} \right) = 82.2 \text{ dB} \quad \blacktriangleright$$

Drill Problems

D7.1 What are the differential- and common-mode gains of the amplifiers of Figure 7.3 if $R_{C1} = R_{C2} = 5 \text{ k}\Omega$ and $R_{EE} = 20 \text{ k}\Omega$? Assume that $V_{CC} = 12 \text{ V}$, $V_{BE} = 0.7 \text{ V}$, $V_T = 26 \text{ mV}$, and $V_{EE} = 12 \text{ V}$.

$$\text{Ans: } A_c = -0.125; A_d = -53.8$$

D7.2 What are the differential- and common-mode gains of the amplifier of Figure 7.6 if $R_{C1} = R_{C2} = 5 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, $V_{EE} = 15 \text{ V}$, $V_{BE} = 0.7 \text{ V}$, and $V_T = 26 \text{ mV}$? Assume that V_{EE}/R_{TH} is a constant-current source with $R_{TH} = 10 \text{ k}\Omega$.

$$\text{Ans: } A_c = -0.25; A_d = -69$$

D7.3 For the constant-current source shown in Figure 7.5, determine R_E , R_1 , and R_2 , where $V_{EE} = 10 \text{ V}$, $I_{EE} = 2 \text{ mA}$, and $V_{BE} = 0.7 \text{ V}$. Also assume that $V_T = 26 \text{ mV}$ and $\beta = 200$.

$$\text{Ans: } R_E = 2.33 \text{ k}\Omega; R_1 = 93 \text{ k}\Omega; R_2 = 93 \text{ k}\Omega$$

7.3 Current Sources, Active Loads, and Level Shifters

In this section we explore alternate methods of simulating a constant-current source to replace the emitter resistor. One type of source was discussed in Section 7.2.3, where a compensated transistor current source was used.

7.3.1 Widlar Current Source

Due to the high gain of an operational amplifier, the bias currents must be small. Typical collector currents are in the range of $5 \mu\text{A}$. Large resistors are often required to maintain small currents, and these large resistors occupy correspondingly large areas on the IC chip. It is therefore often desirable to replace these large resistors with current sources. One such device is the *Widlar current source* [63], as illustrated in Figure 7.8. The two transistors Q_1 and Q_2 are identical. We sum the voltages around the base loop of the two transistors to get

$$V_{BE1} - V_{BE2} - I_{C2}R_2 = 0 \quad (7.13)$$

We saw in Section 3.2 that

$$I_C = \beta I_o \exp\left(\frac{V_{BE}}{V_T}\right)$$

Solving this for V_{BE} yields

$$V_{BE} = V_T \ln\left(\frac{I_C}{\beta I_o}\right) \quad (7.14)$$

Substituting the expression of equation (7.14) into equation (7.13), we obtain

$$V_T \ln\left(\frac{I_{C1}}{\beta I_o}\right) - V_T \ln\left(\frac{I_{C2}}{\beta I_o}\right) - I_{C2}R_2 = 0$$

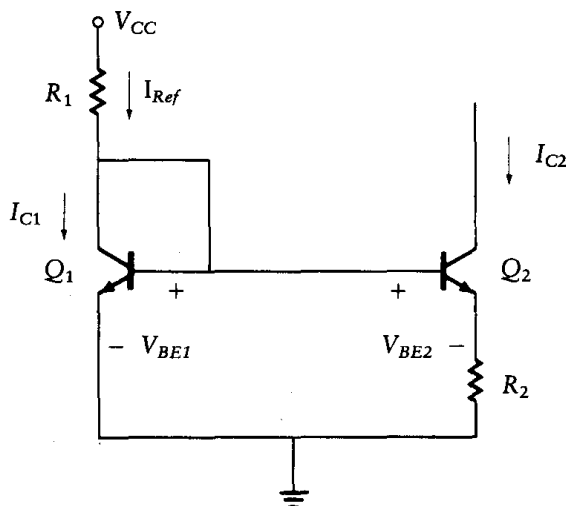


Figure 7.8 Widlar current source.

We assume that the two transistors are matched so that I_o , β , and V_T are the same for both transistors. Thus

$$V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) = I_{C2}R_2 \quad (7.15)$$

For design purposes, I_{C1} is usually known, since it is used as the reference, and I_{C2} is the desired output current. This allows us to solve equation (7.15) for the required value of R_2 .

We use an example to illustrate how a current source can be designed to provide a small constant current while using resistors that are easily fabricated on an IC chip.

Example 7.3 Widlar Current Source (Design)



Design a Widlar current source to provide a constant current of $3 \mu\text{A}$ with $V_{CC} = 12 \text{ V}$, $R_1 = 50 \text{ k}\Omega$, and $V_{BE} = 0.7 \text{ V}$.

SOLUTION Use the circuit of Figure 7.8. Apply KVL to the Q_1 transistor to obtain

$$I_{C1} \approx I_{\text{Ref}} = \frac{12 - 0.7}{50,000} = 0.226 \text{ mA}$$

From equation (7.15) we have

$$0.026 \ln\left(\frac{0.226 \times 10^{-3}}{3 \times 10^{-6}}\right) = 3 \times 10^{-6} R_2$$

and

$$R_2 = 37.5 \text{ k}\Omega$$

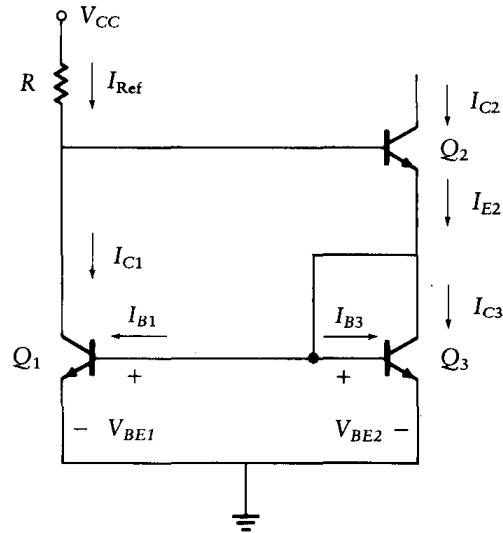


Since R_2 is less than $50 \text{ k}\Omega$, it can be fabricated on an IC.

7.3.2 Wilson Current Source

The *Wilson current source* [65], as shown in Figure 7.9, uses three transistors, and its operation is almost independent of the internal transistor characteristics. Negative feedback from the collector to the base of Q_3 increases the output resistance of this current source.

Figure 7.9
Wilson current source.



We solve for I_{C2} to illustrate the usefulness of this circuit. Applying KCL at the emitter of Q_2 yields

$$I_{E2} = I_{C3} + I_{B3} + I_{B1} \quad (7.16)$$

Using the relationship between collector and base current yields,

$$I_{E2} = I_{C3} \left(1 + \frac{1}{\beta} \right) + \frac{I_{C1}}{\beta} \quad (7.17)$$

Since all three transistors are assumed to be identical,

$$V_{BE1} = V_{BE3}$$

and

$$\beta_1 = \beta_2 = \beta_3$$

With identical transistors, current in the feedback path splits equally between the bases of Q_1 and Q_3 , leading to the result that

$$I_{C1} = I_{C3}$$

Thus, equation (7.17) becomes

$$I_{E2} = I_{C3} \left(1 + \frac{2}{\beta} \right)$$

The collector current of Q_2 is

$$I_{C2} = \frac{I_{E2}\beta}{\beta + 1} = \frac{I_{C3}(1 + 2/\beta)\beta}{\beta + 1}$$

Solving for I_{C3} yields

$$I_{C3} = \frac{I_{C2}}{(1 + 2/\beta)\beta/(1 + \beta)} = I_{C2} \frac{\beta + 1}{\beta + 2} \quad (7.18)$$

Summing currents at the base of Q_2 , we find

$$I_{C1} = I_{\text{Ref}} - \frac{I_{C2}}{\beta}$$

or

$$I_{C2} = \beta(I_{\text{Ref}} - I_{C1}) \quad (7.19)$$

Since $I_{C1} = I_{C3}$, we substitute I_{C3} from equation (7.18) for I_{C1} in equation (7.19) to get

$$I_{C2} = \beta I_{\text{Ref}} - \frac{\beta(\beta + 1)}{\beta + 2} I_{C2}$$

and solving for I_{C2} ,

$$\begin{aligned} I_{C2} &= \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} I_{\text{Ref}} \\ &= \left(1 - \frac{2}{\beta^2 + 2\beta + 2}\right) I_{\text{Ref}} \end{aligned} \quad (7.20)$$

Equation (7.20) shows that β has little effect upon I_{C2} , since, for reasonable values of β ,

$$\frac{2}{\beta^2 + 2\beta + 2} \ll 1$$

7.3.3 Current Mirrors

The circuit shown in Figure 7.10 is known as a *current mirror*. It is used in op-amp circuit design to reproduce a current from one location to one or more other locations. In this circuit, Q_2 is in the linear mode, since the collector

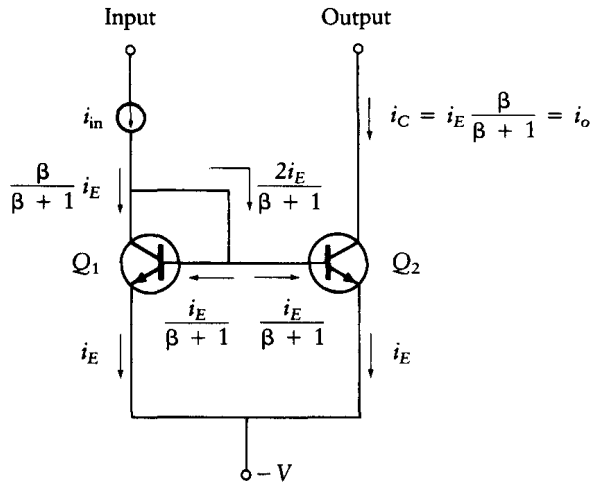


Figure 7.10 Current mirror.

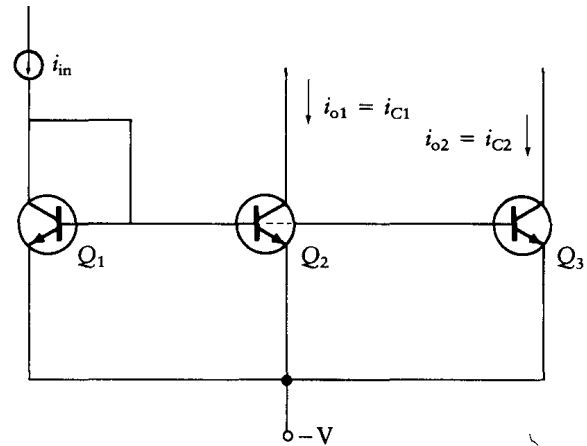


Figure 7.11 Multiple-current mirrors.

voltage (output) is higher than the base voltage. The transistors Q_1 and Q_2 are identical devices fabricated on the same IC chip. The emitter currents are equal, since the emitters and bases are in parallel. If we sum the currents of Q_2 , we obtain

$$i_B + i_C = i_E$$

so

$$i_o = i_C = i_E - \frac{i_E}{\beta + 1} = \frac{\beta i_E}{\beta + 1}$$

Summing currents at the collector of Q_1 yields

$$i_{in} = \left(\frac{\beta}{\beta + 1} + \frac{2}{\beta + 1} \right) i_E = \frac{\beta + 2}{\beta + 1} i_E$$

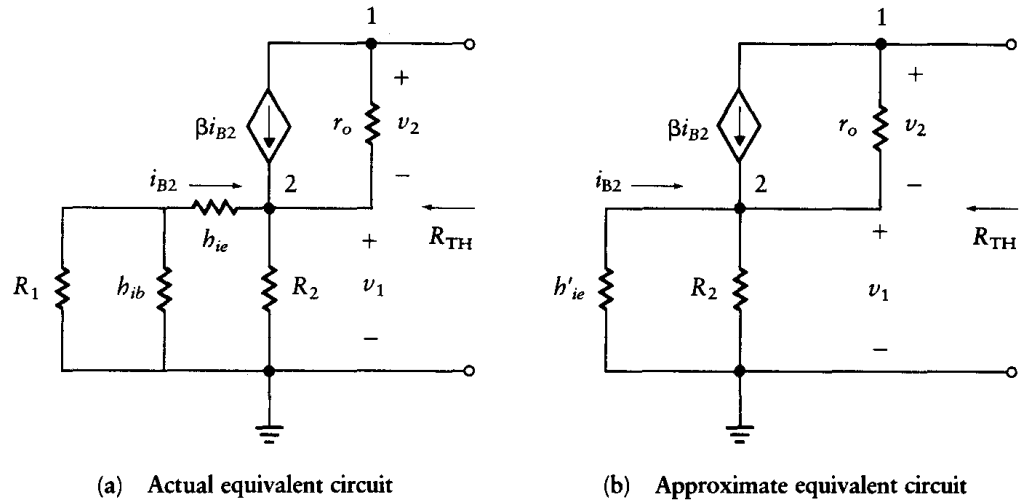
The current gain of the mirror is given by

$$A_i = \frac{i_o}{i_{in}} = \frac{\beta i_E}{\beta + 1} \frac{\beta + 1}{(\beta + 2)i_E} = \frac{1}{1 + 2/\beta} \approx 1$$

If β is much larger than 1, this current gain is approximately equal to unity, and the current mirror has reproduced the input current.

This concept is extended to several other circuits, as shown in Figure 7.11. The current input of Q_1 is mirrored into several other transistors, Q_2, Q_3, \dots ,

Figure 7.12
Widlar current-source equivalent circuit.



Q_n . The errors in base current accumulate when multiple outputs are used, and the current gain tends to deviate from unity.

7.3.4 Current Sources as Active Loads

In the conventional differential amplifiers of Section 7.2, the collector loads consist of resistors. The differential gain is

$$A_v = \frac{v_o}{v_i} = \frac{-R_C}{h_{ib}} = \frac{-R_C I_{CQ}}{V_T}$$

In order to achieve a large voltage gain, the product $R_C I_{CQ}$ must be large. This requires large values of either resistance or power supply voltage. Since the power supply size is usually fixed, large resistors are required. The preceding sections illustrate several alternate forms of almost-ideal constant-current sources. We now show that these are equivalent to large resistors.

The Widlar circuit can be used to simulate a high resistance. The small-signal equivalent circuit is shown in Figure 7.12. Since this circuit has no independent sources, it is equivalent to a single Thevenin resistance. To find the value of this resistance, we assume a current, i_{TH} , find the resulting voltage, and take the ratio. We start by summing currents at node 1,

$$i_{TH} = \beta i_{B2} + \frac{v_2}{r_o} \tag{7.21}$$

and at node 2,

$$\beta i_{B2} + \frac{v_2}{r_o} - \frac{v_1}{R_2} + i_{B2} = 0 \quad (7.22)$$

From equation (7.21), we have

$$v_2 = (i_{TH} - \beta i_{B2})r_o \quad (7.23)$$

Also

$$v_1 = -i_{B2}h'_{ie} \quad (7.24)$$

where

$$h'_{ie} = h_{ie} + (h_{ib}||R_1)$$

Substituting equations (7.23) and (7.24) into equation (7.22) yields

$$-i_{TH} = i_{B2} \left(1 + \frac{h'_{ie}}{R_2} \right) \quad (7.25)$$

Using the relationship

$$R_{TH} = \frac{v_{TH}}{i_{TH}}$$

yields

$$R_{TH} = \frac{r_o(1 + \beta + h'_{ie}/R_2) + h'_{ie}}{1 + h'_{ie}/R_2}$$

Since

$$r_o \gg h'_{ie}$$

we have

$$R_{TH} = r_o \left[\frac{1 + \beta + h'_{ie}/R_2}{1 + h'_{ie}/R_2} \right] = r_o \left[1 + \frac{\beta}{1 + h'_{ie}/R_2} \right]$$

In order to simplify this result, assume that

$$\frac{h'_{ie}}{R_2} \gg 1$$

and

$$h_{ie} = \frac{\beta V_T}{I_{CQ}}$$

Then

$$\begin{aligned} R_{TH} &= r_o \left[1 + \frac{\beta}{h_{ie} R_2} \right] \\ &= r_o \left[1 + \frac{\beta R_2 I_{CQ}}{\beta V_T} \right] \end{aligned}$$

Finally,

$$R_{TH} = r_o \left[1 + \frac{I_{CQ} R_2}{V_T} \right] \quad (7.26)$$

Equation (7.26) shows that R_{TH} depends upon $I_{CQ} R_2$, which is the dc voltage drop across R_2 . The larger the voltage drop, the higher the output resistance. Generally, the output resistance of a simple current source is increased by the addition of resistances (R_2 in Figures 7.8 and 7.12) in the emitters of the current-source transistors.

We perform a similar analysis for the Wilson current source. This analysis is like that used for the Widlar source, so we simply state the result here. The equivalent resistance is given by

$$R_{TH} = \frac{\beta r_o}{2} \quad (7.27)$$

We now examine two applications of the constant-current circuits. Figure 7.13(a) illustrates a CE amplifier with an active load as the collector resistor. In Figure 7.13(b), a differential amplifier is shown using active loads, Widlar current sources, and current mirrors. Similar circuits of this type are found in many ICs, since large resistors are avoided in the fabrication process. Transistors Q_1 and Q_2 are the differential-amplifier transistors, Q_3 and Q_4 are the active loads for the amplifier, Q_3 , Q_4 , and Q_6 form the current source with current mirrors, and Q_5 and Q_7 form a Widlar current source.

7.3.5 Level Shifters

Amplifiers often produce dc voltages at the output. Even if the input has an average value of 0 V, the output usually has a nonzero average voltage due to

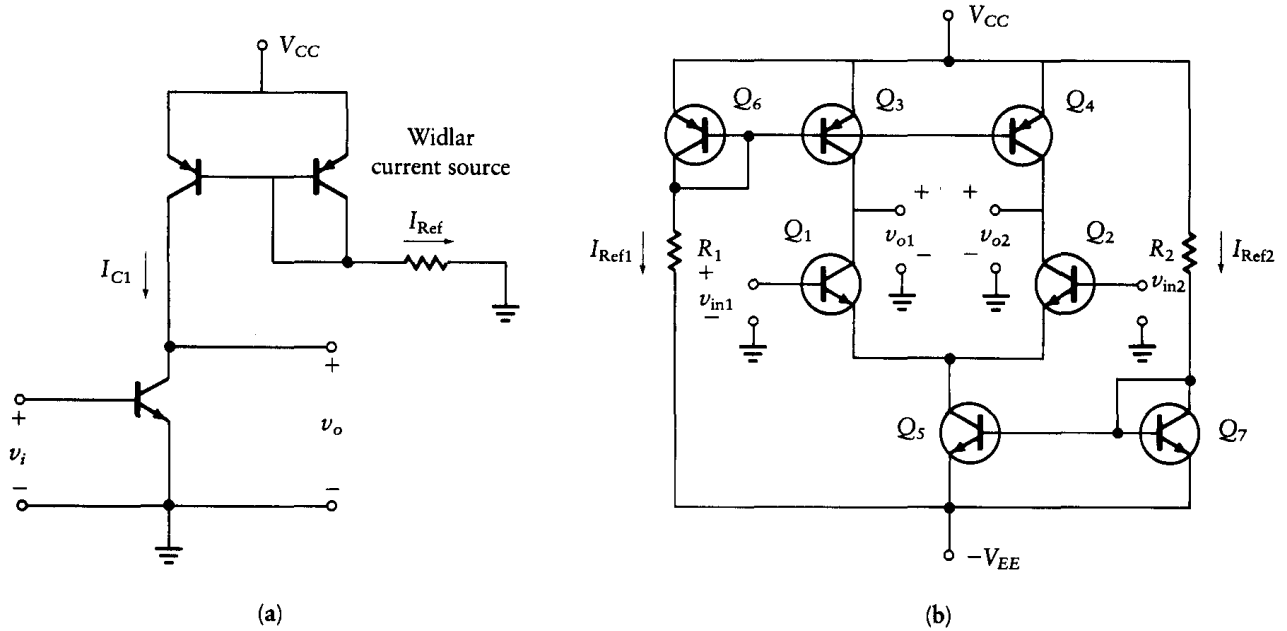


Figure 7.13 CE amplifier with active load.

biasing effects. These dc voltages can cause difficulties at the output, since they cause an undesired offset.

In Chapter 6 we study the Class B power amplifier, which provides a method of reducing the offset voltages in the output stage. However, we cannot always use Class-B amplifiers, so another technique is necessary. *Level shifters* are amplifiers that add or subtract a known voltage from the input in order to compensate for dc offset voltages.

Since the op-amp is a multistage dc amplifier with high gain, unwanted dc voltages are always a source of concern. That is, a small offset in an early stage can saturate a later stage. For this reason level shifters are included in the design of op-amps.

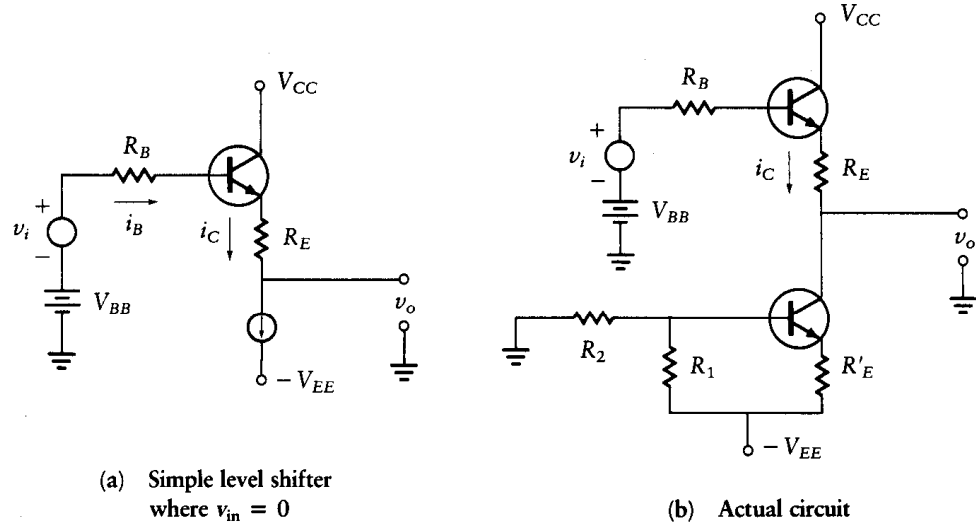
Figure 7.14 illustrates a simple level shifter. We show that this shifter acts as a unit-gain amplifier for ac while providing an adjustable dc output. We begin the analysis by using KVL in Figure 7.14(a) and letting $v_i = 0$ to get

$$V_{BB} = I_B R_B + V_{BE} + I_C R_E + V_o$$

Since

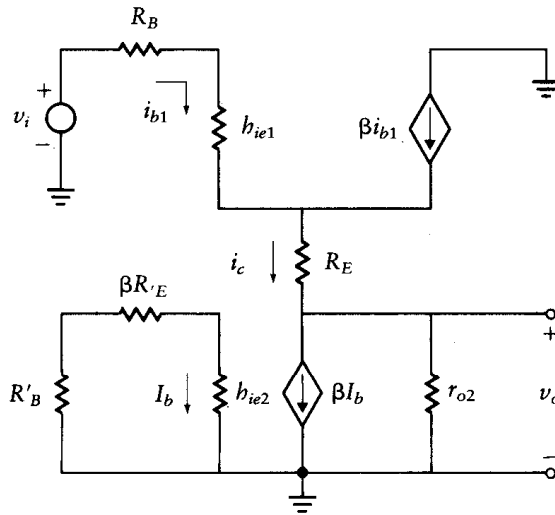
$$I_B = \frac{I_C}{\beta}$$

Figure 7.14
Level shifter.



(a) Simple level shifter where $v_{in} = 0$

(b) Actual circuit



(c) Small-signal ac equivalent circuit

we solve for the dc value of output voltage, V_o :

$$V_o = V_{BB} - \frac{R_B I_C}{\beta} - I_C R_E - V_{BE} \tag{7.28}$$

This equation shows that by selecting a value of R_E , V_o can be set to any desired dc level less than $V_{BB} - V_{BE}$. Since V_{BB} is the dc level acquired from the previous stage, this amplifier is used to shift the level *downward* (to a lower value). If *upward* shifting is required, a similar circuit is used, but *npn* transis-

tors are substituted for the *npn* transistors. A complete circuit with active current sources is shown in Figure 7.14(b).

We examine small-signal ac signals. Figure 7.14(c) illustrates the ac equivalent circuit. Note that βI_B is the collector current in the active current source, and we assume it to be a constant. Because the ac value of the current is zero, this current source is replaced by an open circuit in the following equations. We write the ac equations using KVL:

$$v_i = i_{b1}R_B + i_{b1}h_{ie1} + i_cR_E + v_o \quad (7.29)$$

and

$$v_o = i_c r_{o2}$$

$$i_c = \frac{v_o}{r_{o2}}$$

$$v_{in} = \frac{v_o R_B}{\beta r_{o2}} + \frac{v_o h_{ie1}}{\beta r_{o2}} + \frac{v_o R_E}{r_{o2}} + v_o$$

Finally, the ratio of ac output to ac input is

$$\frac{v_o}{v_i} = \frac{1}{1 + (R_B/\beta + h_{ie}/\beta + R_E)/r_{o2}} \quad (7.30)$$

Equation (7.30) shows that as r_{o2} becomes large, the ratio of output to input approaches unity, and the level shifter acts like an emitter follower to ac. This is the desired result.

Example 7.4



Two direct-coupled CE amplifiers are placed in series to achieve the desired voltage gain. Design a level shifter to be placed in between the two CE amplifiers to provide a dc voltage sufficiently low to prevent the second CE amplifier from saturating. Do this by providing a 1 V bias to the second stage. The collector voltage, V_C , of the first amplifier is 4 V, and the R_C of that amplifier is 1 k Ω . Design the level shifter to have an I_{CQ} of 1 mA using dc power of ± 10 V. Use a current source of the type shown in Figure 7.5 with transistors having $\beta = 100$, $V_{BE} = 0.7$ V, and $V_\gamma = 0.7$ V.

SOLUTION The level shifter is shown in Figure 7.14(b). We need to find the values of R_E , R_1 , R_2 , and R'_E . Since the first amplifier has a V_C of 4 V, the