BASIC OF ELECTRONICS

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Bipolar Transistors

- 2.3 Transistor Characteristic curves
- 2.5 The CE Amplifier with/ without Emitter Resistor
  - 2.5.2 Introduction to Analysis
  - 2.5.3 Introduction to Design

2.3 Transistor Circuits- Characteristic curves

Transistor characteristic curves are parametric curves of i_C versus v_{CE}, where i_B is a parameter. Figure 2.11 shows an example of a family of such curves. Each transistor type has its own unique set of characteristic curves.

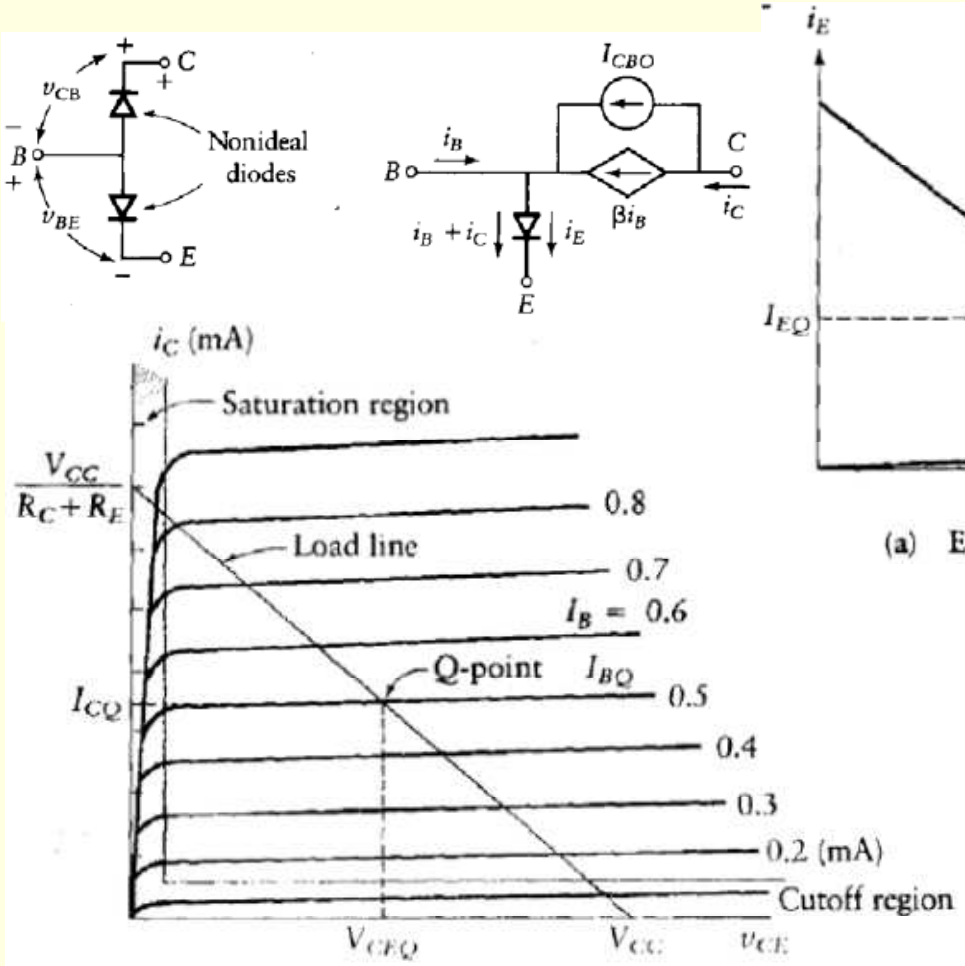
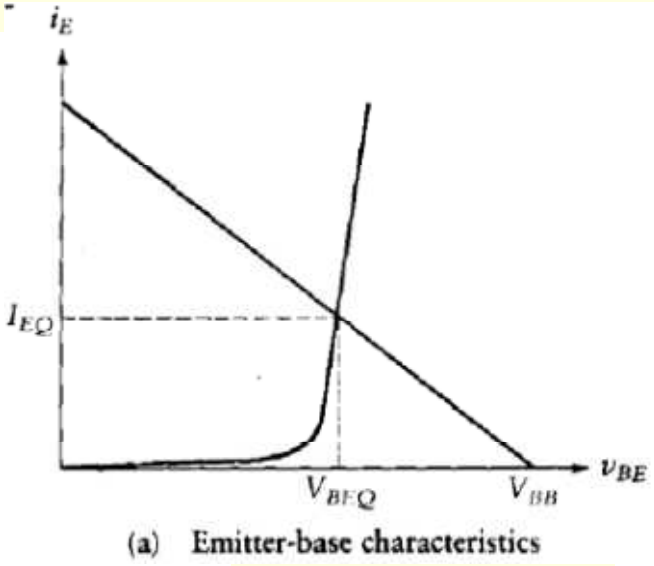


Figure 2.11 Family of transistor characteristic curves.



(a) Emitter-base characteristics

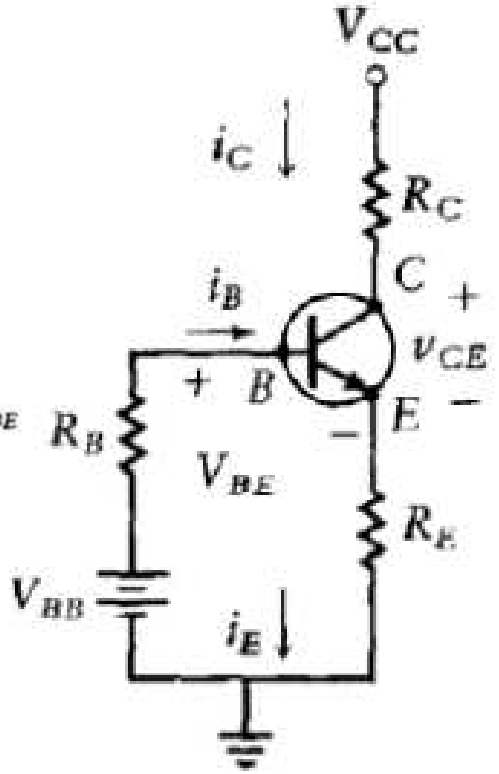


Figure 2.12 Simple transistor circuit.

2.3 Transistor Circuits- Characteristic curves

As an example of the use of the characteristic curves, we shall analyze the circuit of Figure 2.12. Applying KVL around the collector to emitter loop, we obtain

$$V_{CC} = i_C R_C + v_{CE} + i_E R_E \tag{2.7}$$

Since i_E is approximately equal to i_C, equation (2.7) can be simplified, as in equation (2.8).

$$V_{CC} = i_C(R_C + R_E) + v_{CE} \tag{2.8}$$

Equation (2.8) defines a straight-line relationship between i_C and v_{CE}. That is,

$$i_C = \frac{V_{CC} - v_{CE}}{R_C + R_E} = -\frac{1}{R_C + R_E} v_{CE} + \frac{V_{CC}}{R_C + R_E} \tag{2.9}$$

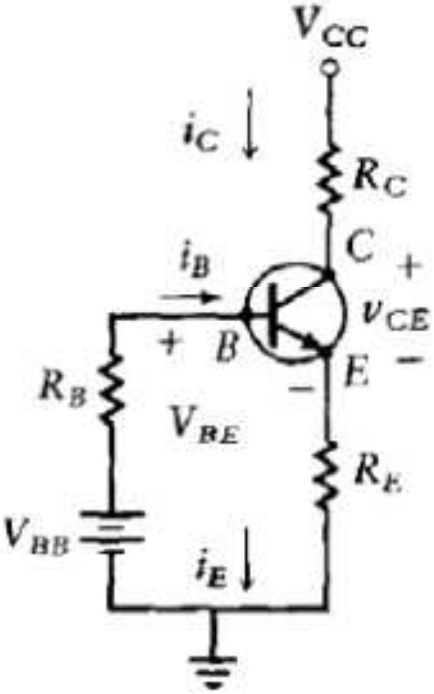


Figure 2.12 Simple transistor circuit.

One way to plot this straight line is to solve for the two axis intercepts. If $i_C = 0$, $v_{CE} = V_{CC}$. If $v_{CE} = 0$, then

The dc load line is plotted on the characteristic curves When we discuss design, we will see how properly to select the circuit parameters.

2.5 The CE Amplifier

The CE, or common emitter transistor amplifier, is so called because the base and collector current combine in the emitter. Figure 2.13 shows the configuration of the amplifier, where an *npn* transistor has been selected for illustration.

We first analyze the circuit of Figure 2.13 under dc conditions. The variable source, v_s, is set equal to zero. KVL around the base loop is written as follows:

$$I_B R_B + V_{BE} - V_{BB} = 0 \qquad (2.10)$$

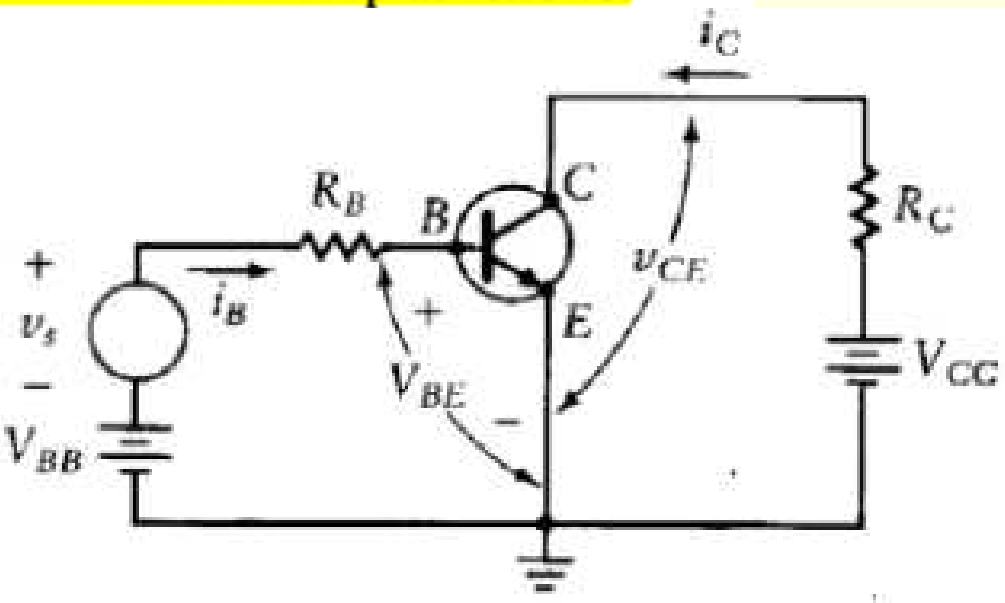
Recall that V_{BE} is equal to 0.6 to 0.7 V for silicon transistors, we use 0.7 V unless otherwise specified.

We now write the KVL around the collector-emitter loop as follows:

$$V_{CC} = R_C I_C + V_{CE}$$

Then

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \qquad (2.11)$$

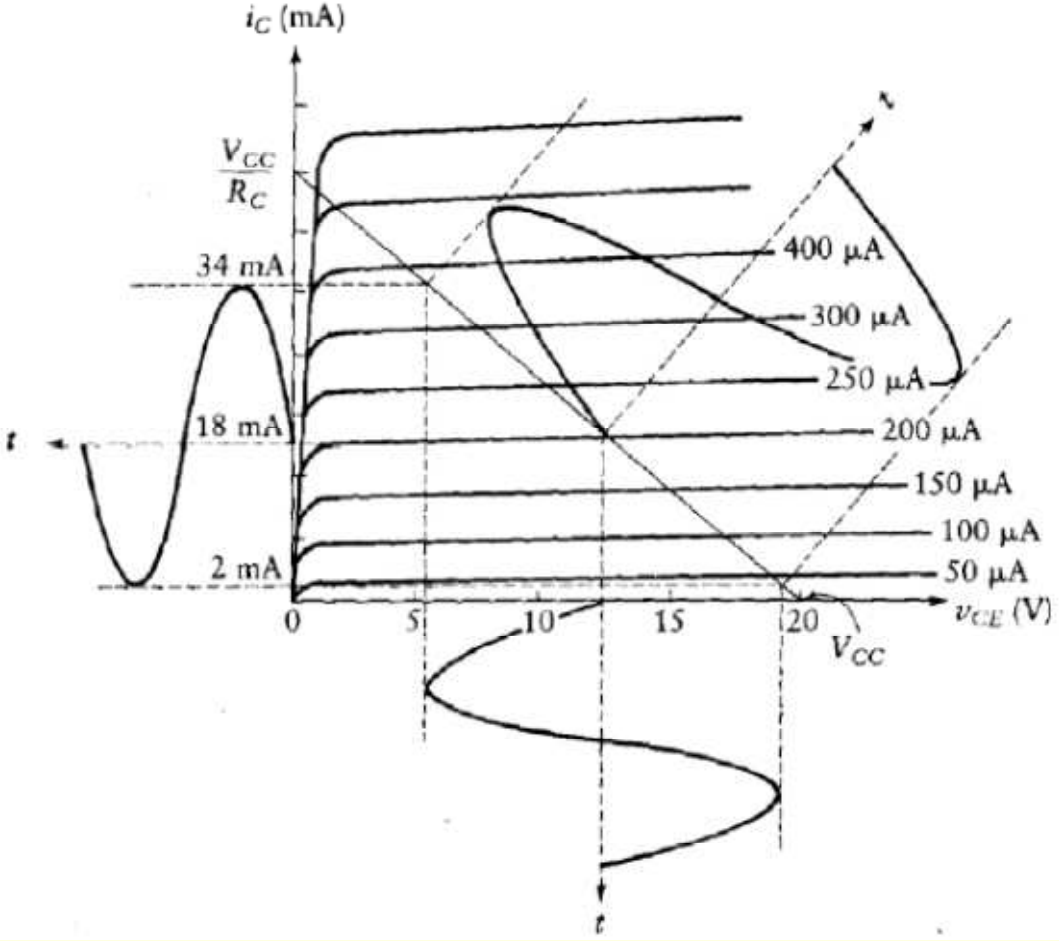


2.5 The CE Amplifier

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \qquad (2.11)$$

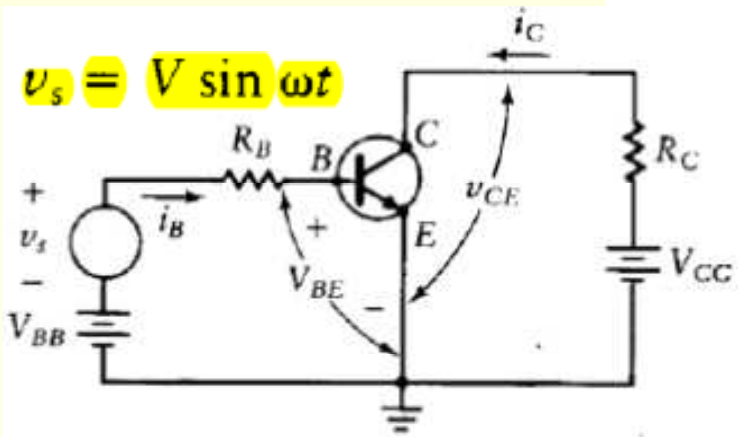
Equation (2.11) defines the load line, which is drawn on the characteristic curves in Figure 2.14(a). A Q-point, or operating point, which is defined as the zero-signal point, can now be selected to lie on the load line. Now if we assume an ac input of

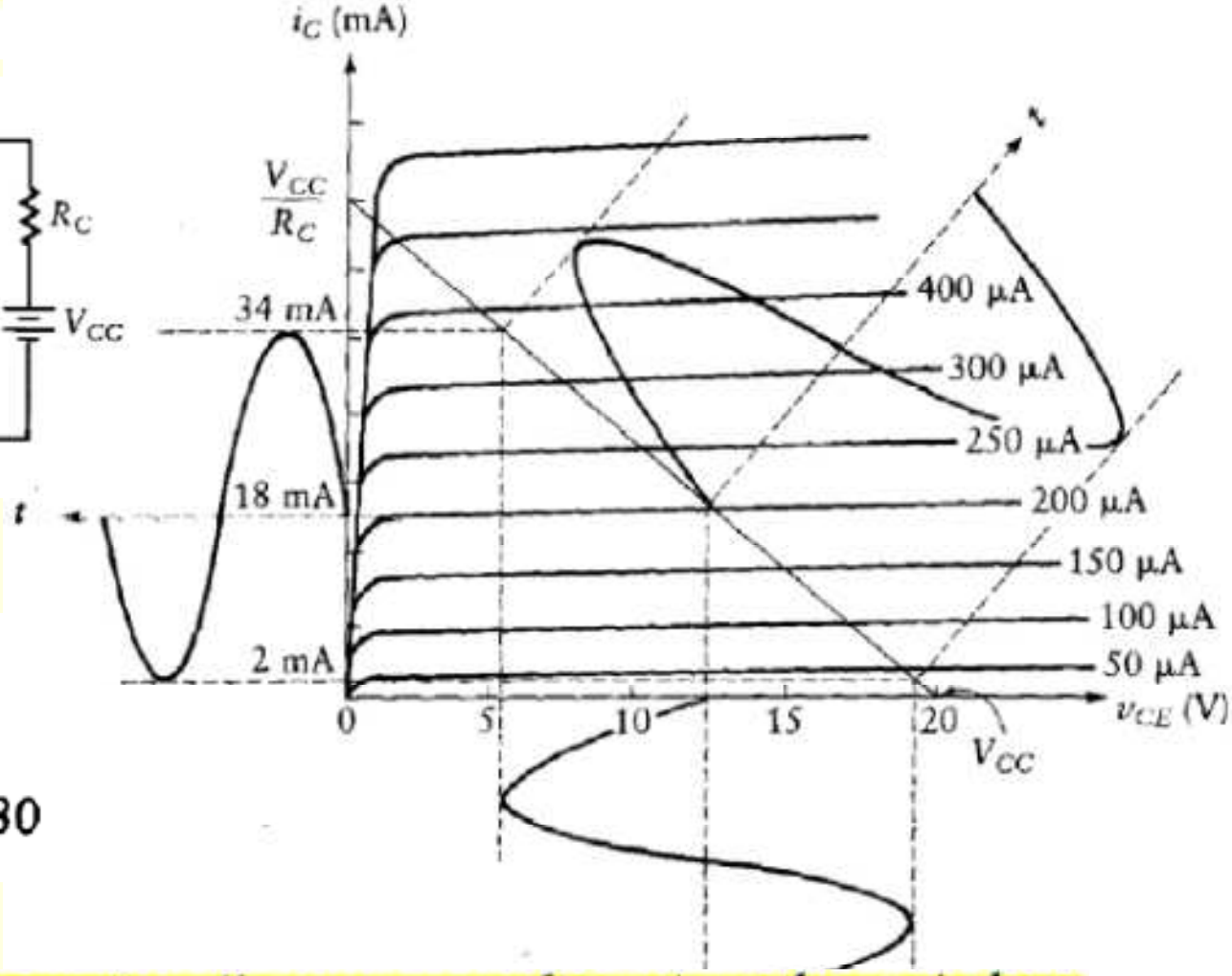
$$v_s = V \sin \omega t$$



2.5 The CE Amplifier

the output wave can be found graphically. By moving the operating point up and down along the load line as i_B varies, we can plot i_C, i_B, and v_{CE}, as shown in Figure 2.14.



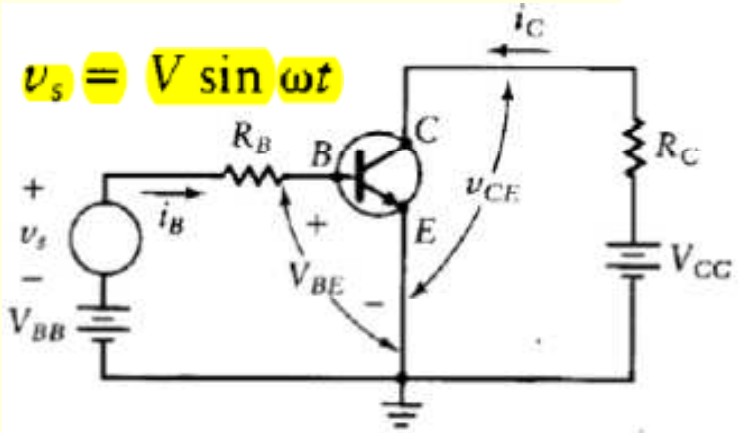


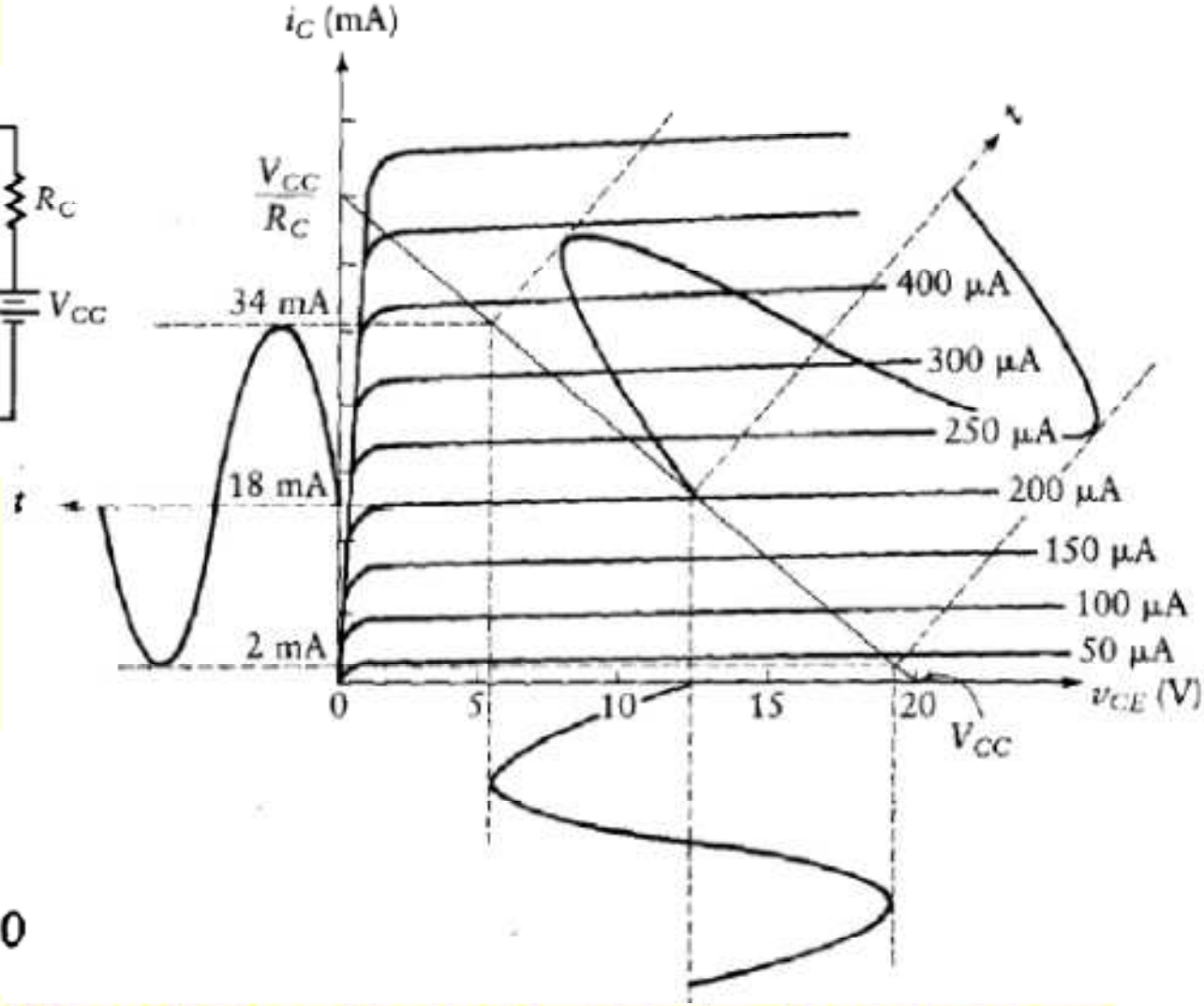
$$A_i = \frac{\Delta i_C}{\Delta i_B}$$

$$= \frac{32 \text{ mA}}{400 \ \mu\text{A}} = 80$$

Let us determine the change in collector current for a given change in base current. This ratio is the *current gain*, which is defined as

2.5 The CE Amplifier





$$A_i = \frac{\Delta i_C}{\Delta i_B}$$

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Δi_C and Δi_B are read from Figure 2.14 as the total swings in these parameter values. It is this gain that makes the device important for many engineering applications.

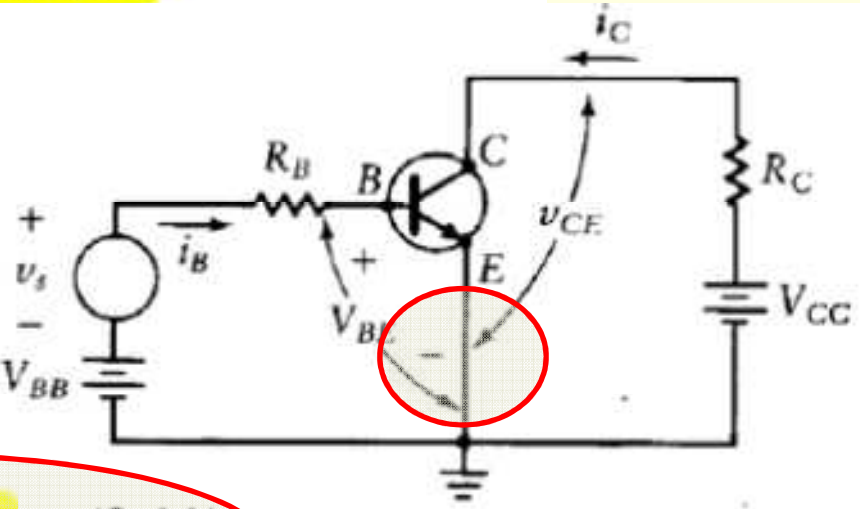
2.5 CE Amplifier with Emitter Resistor

Figure 2.15 illustrates a CE circuit to which an emitter resistor has been added. We write the Kirchhoff equations around the emitter-collector loop to determine the dc load line. Referring to Figure 2.15(a), we find

$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$

Since I_C is approximately equal to I_E, we have

$$I_C = \frac{V_{CC} - V_{CE}}{R_E + R_C} \qquad (2.12)$$



$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \qquad (2.11)$$

If $I_C = 0$, then

$$V_{CE} = V_{CC}$$

This operating point is in the cutoff region. If $V_{CE} = 0$, we have

$$I_C = \frac{V_{CC}}{R_E + R_C}$$

This operating point is in the saturation region. The resulting load line is as drawn in Figure 2.15(b).

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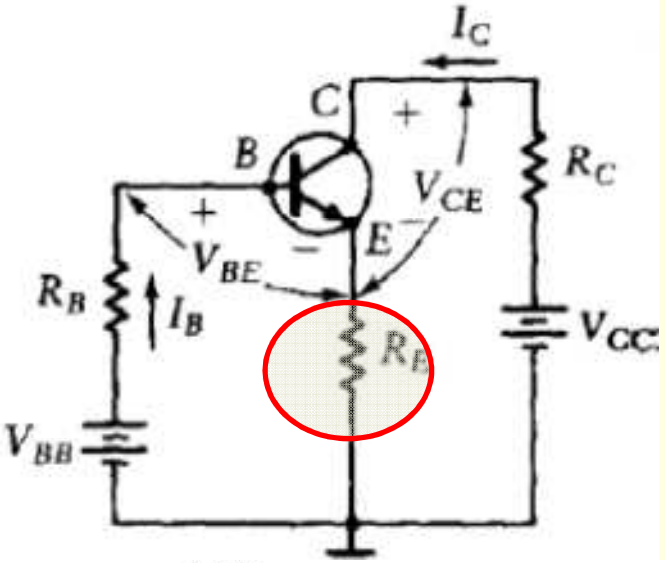

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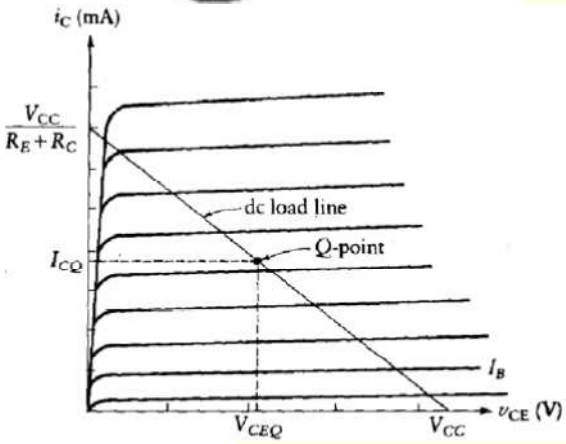
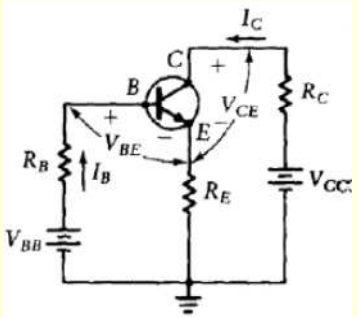


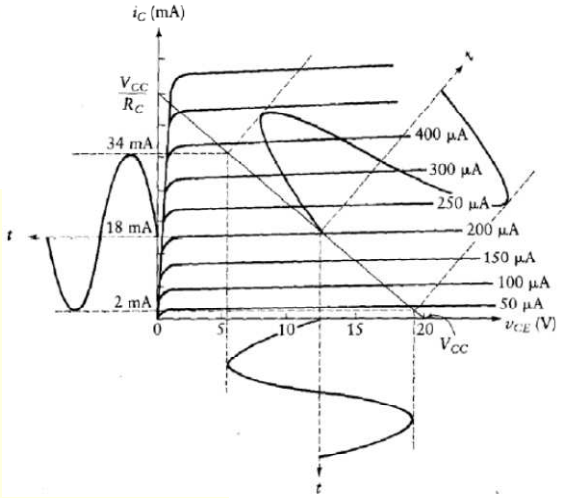
This operating point is in the saturation region. The resulting load line is as drawn in Figure 2.15(b).

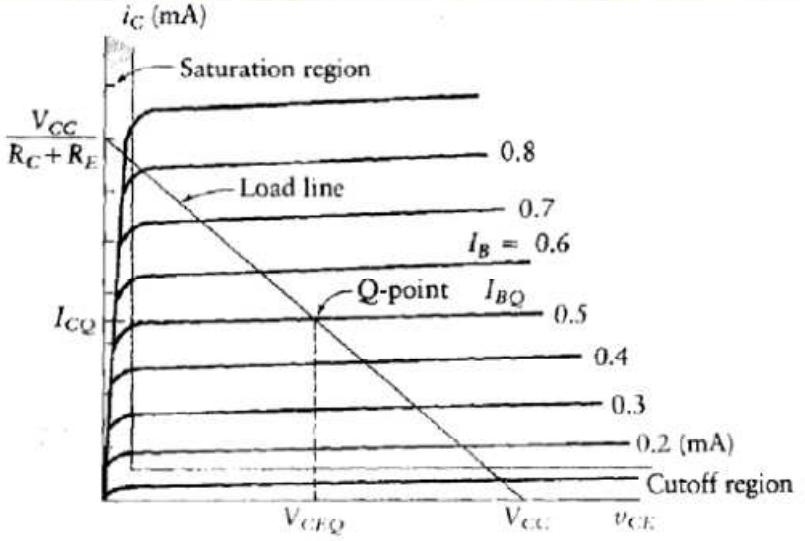
2.5 CE Amplifier with Emitter Resistor

In using the common emitter transistor, we avoid the nonlinear region of the characteristic curves occurring at low values of i_C (cutoff) and at low values of v_{CE} (saturation). In designing a transistor amplifier, we often desire maximum undistorted output swing. If the ac input signal is symmetrical about zero, we can achieve maximum swing by placing the Q-point in the center of the load line. Thus,

$$V_{CEQ} = \frac{V_{CC}}{2}$$







This equation establishes V_{CEQ} and I_{CQ}. Additionally, since the base-emitter junction acts as a diode,

$$V_{BE} = V_\gamma$$

2.5 CE Amplifier with Emitter Resistor

Writing KVL equations around the base loop, we obtain

$$V_{BB} = R_B i_B + v_{BE} + i_C R_E$$

Note that we are using lowercase letters and uppercase subscripts for the variables. This indicates total (dc + ac) values. Because

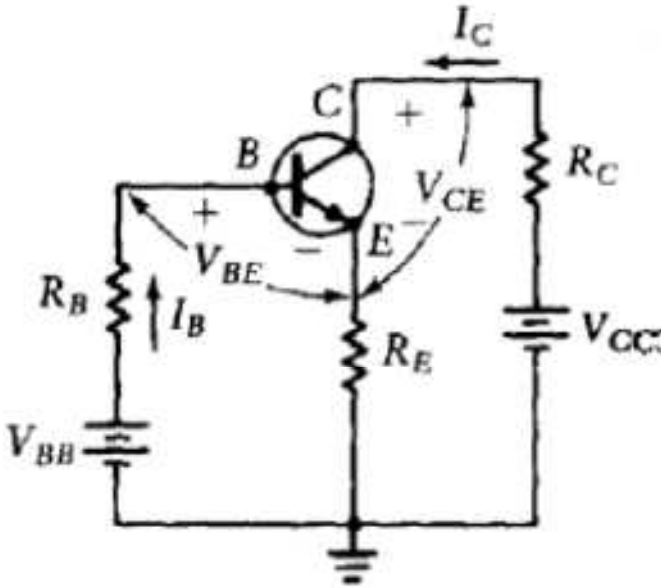
$$i_C = \beta i_B$$

we have

$$V_{BB} = \frac{R_B i_C}{\beta} + V_{BE} + i_C R_E$$

and at the quiescent point,

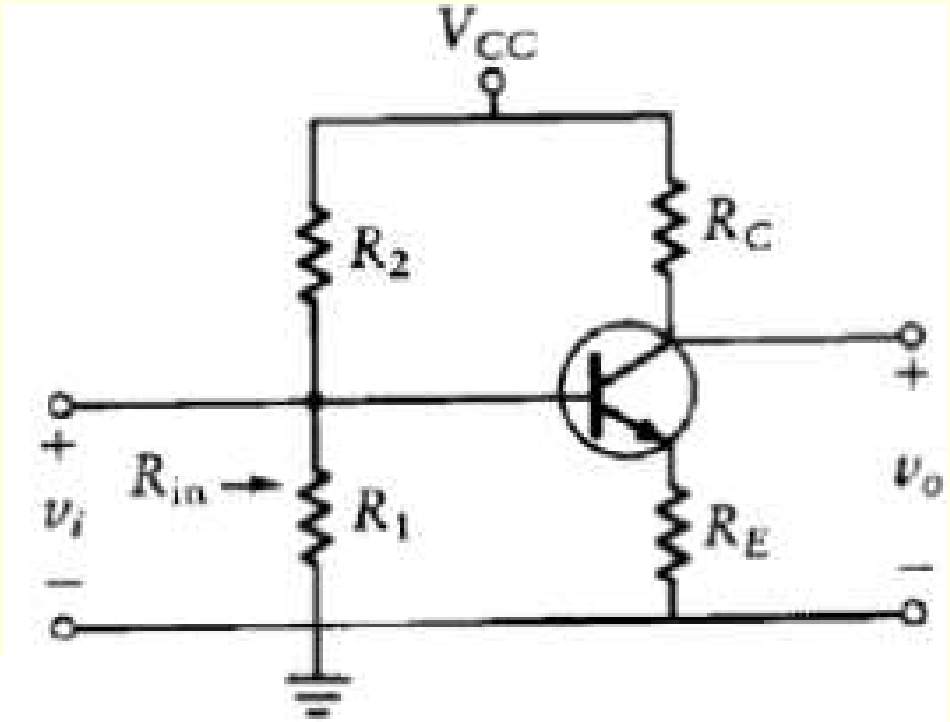
$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} \qquad (2.13)$$

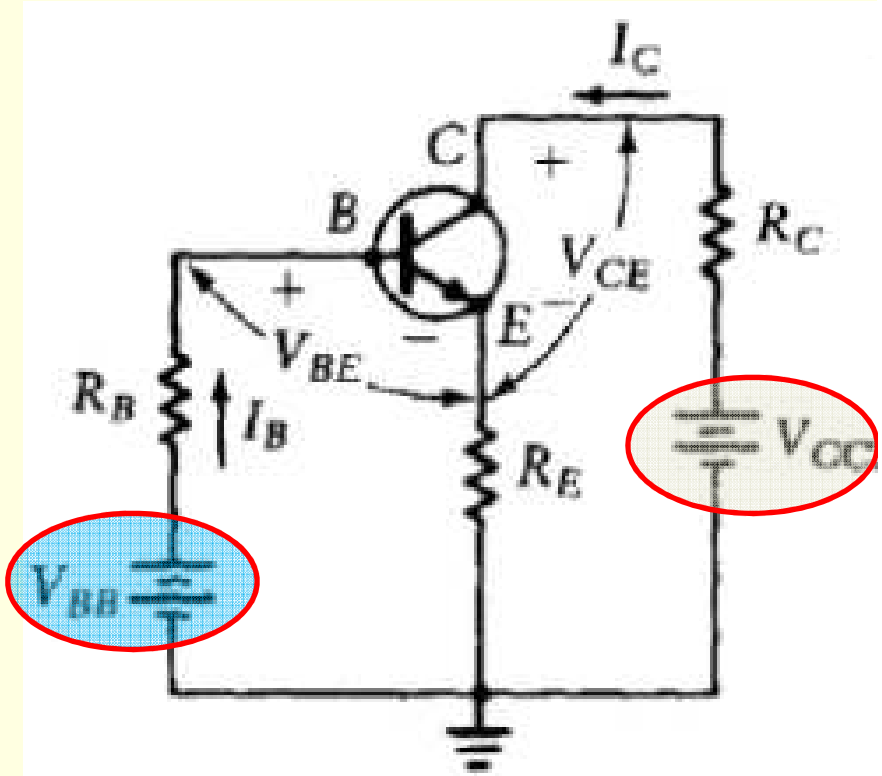


The voltage, V_{BE}, is considered to be a constant at room temperature (25°C) and has a value of about 0.7 V for silicon transistors.

2.5 CE Amplifier with Emitter Resistor

In order to avoid using two separate dc sources, a voltage-divider network can be used to provide the dc source for the base circuit, as shown in Figure 2.16. The values for R_1 and R_2 determine the location of the Q-point. If the resistor and source combination connected to the base in Figure 2.16 is replaced by a Thevenin equivalent, the new circuit is identical to that of Figure 2.15.





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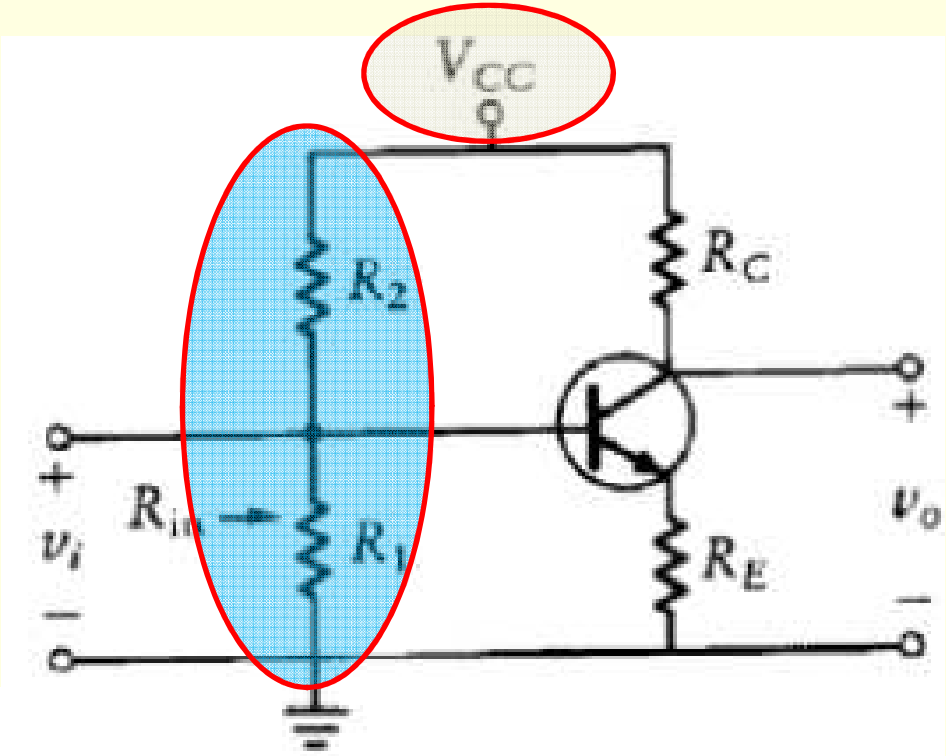

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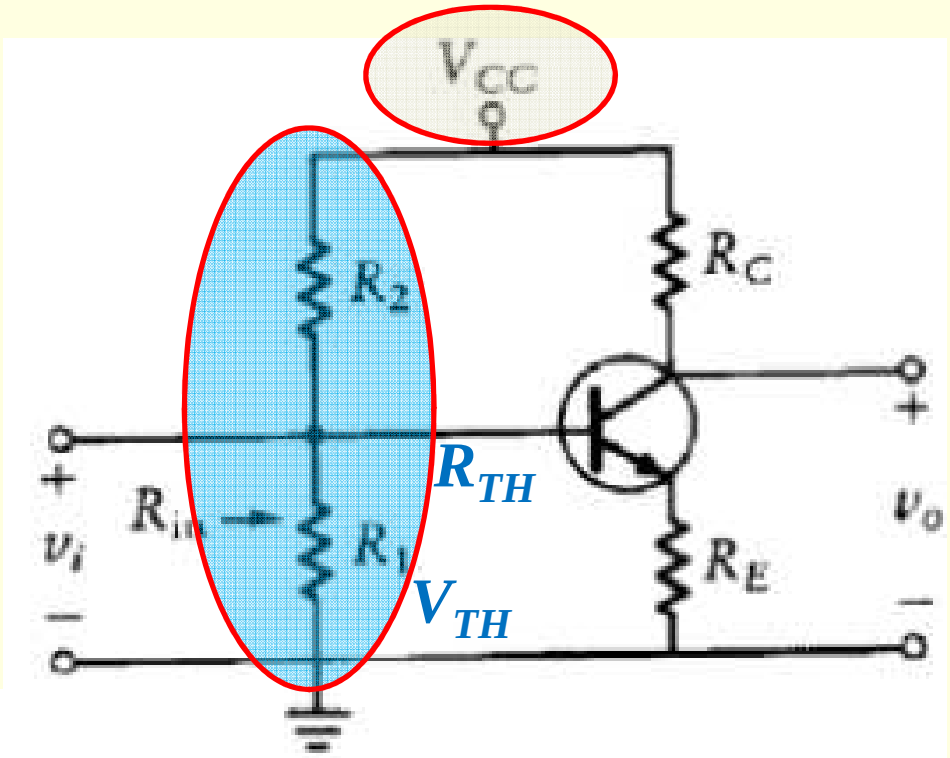
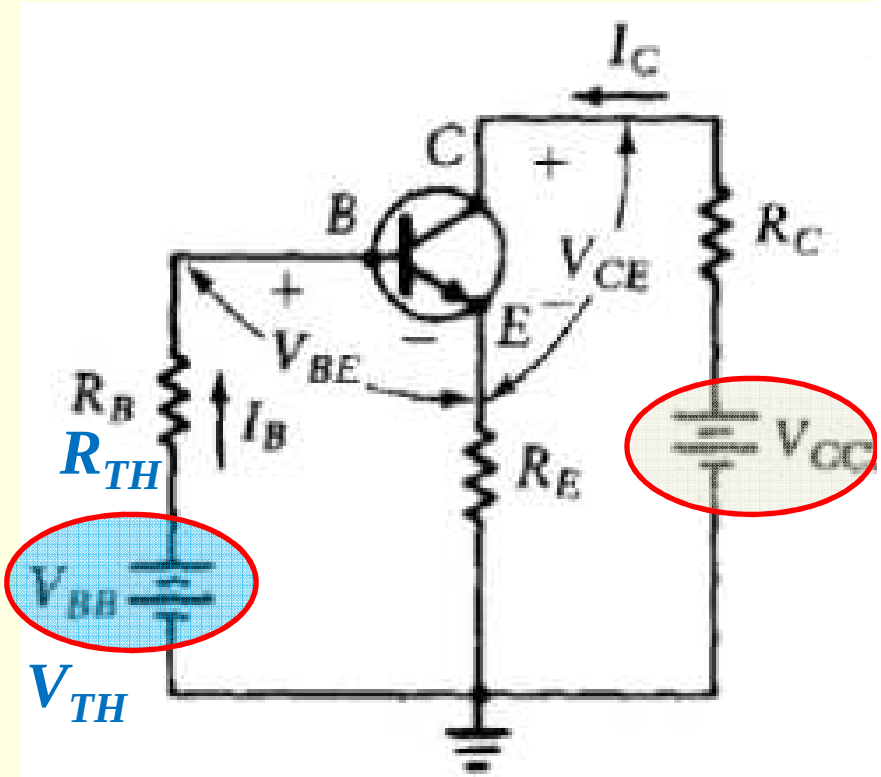


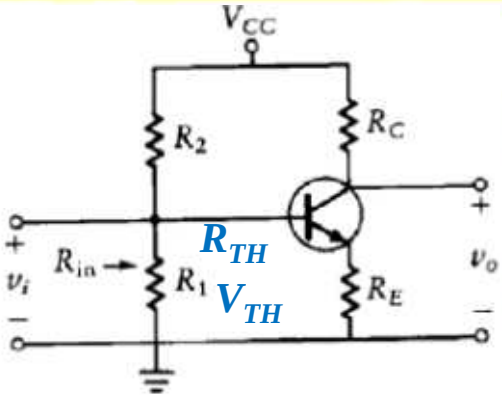


2.5 CE Amplifier with Emitter Resistor

The Thevenin equivalent voltage and resistance from base to ground are

$$V_{TH} = V_{BB} = \frac{R_1 V_{CC}}{(R_1 + R_2)} \tag{2.14}$$

$$R_{TH} = R_1 \parallel R_2 = R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{2.15}$$



We can solve for R_1 and R_2 by substituting equation (2.14) into equation (2.15):

$$R_1 = \frac{R_B V_{CC}}{V_{CC} - V_{BB}} = \frac{R_B}{1 - V_{BB}/V_{CC}} \tag{2.16}$$

$$R_2 = \frac{V_{CC} R_B}{V_{BB}} \tag{2.17}$$

R_1 and R_2 need to be determined to establish the required bias point. The analysis of the previous section assumes that the collector current is equal to the emitter current. This is a good approximation, since β is usually greater than 100.

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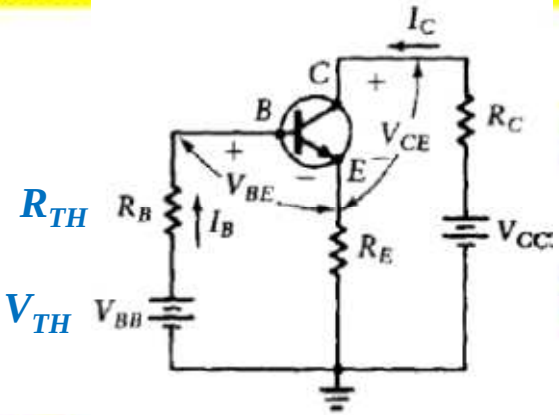

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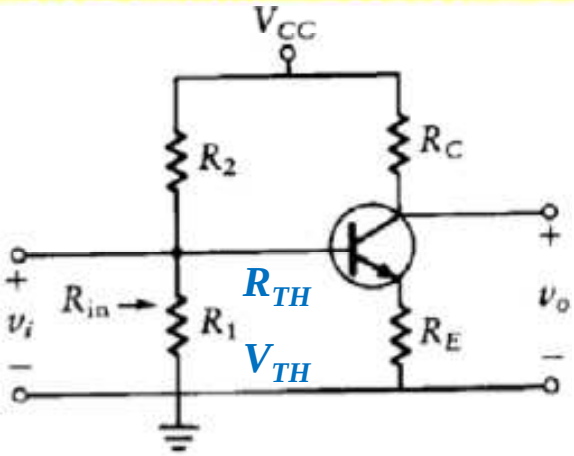

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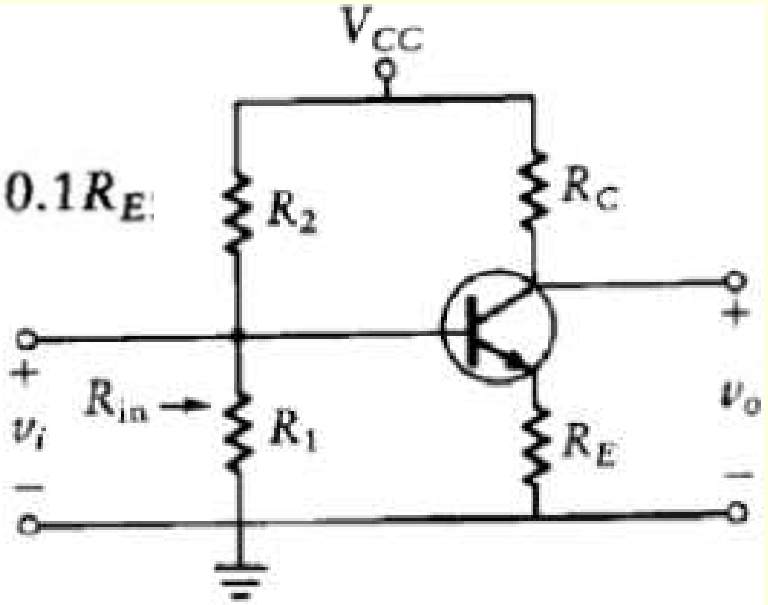
2.5 CE Amplifier with Emitter Resistor

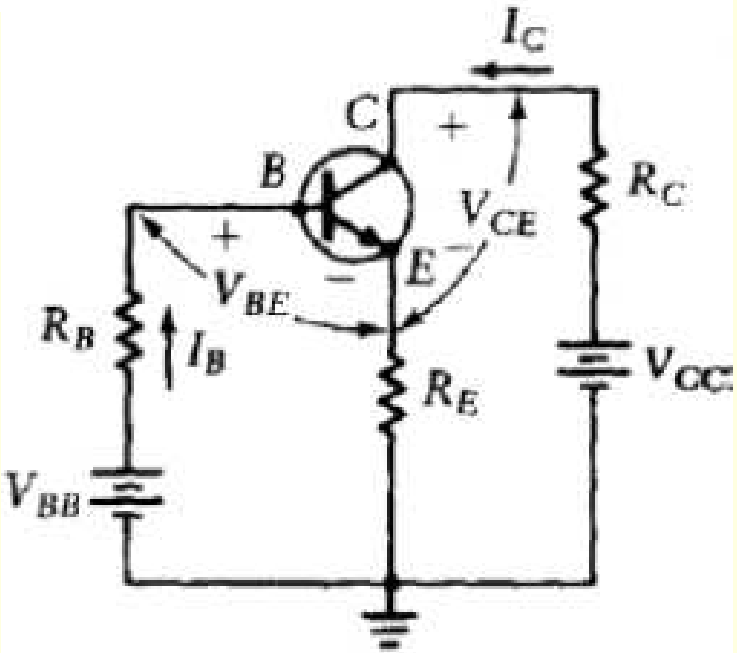
For the circuit under consideration, we wish to have about 10% of the input current going into the base and about 90% shunted through the equivalent external resistor, R_B. This provides bias stability and also permits the use of the simplified equations. Hence, the current in R_B should be about 10 times the base current. To achieve this, we set

$$R_B \leqslant 0.1\,\beta R_E \tag{2.18}$$

or

$$\frac{R_B}{\beta} \leqslant 0.1 R_E$$





This prevents variation in β from significantly affecting the dc operating point of the stage.

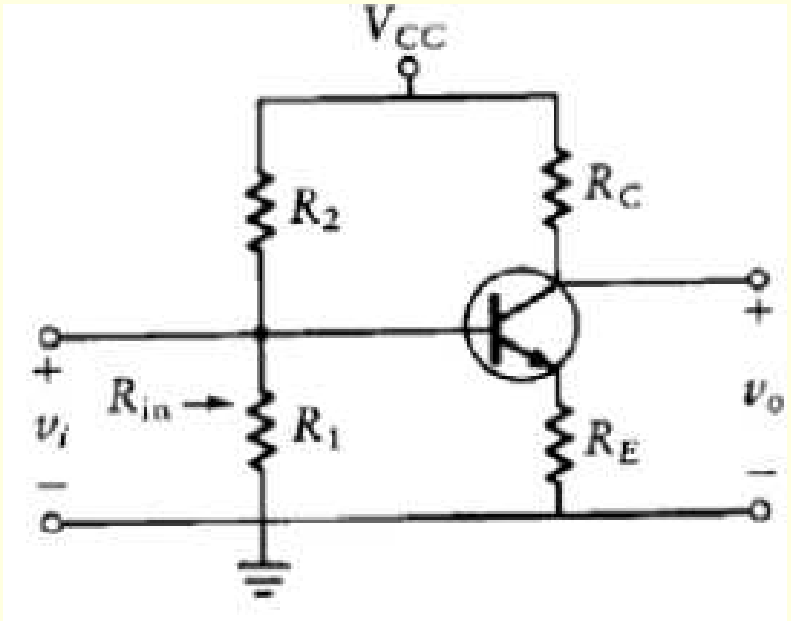
2.5 CE Amplifier with Emitter Resistor

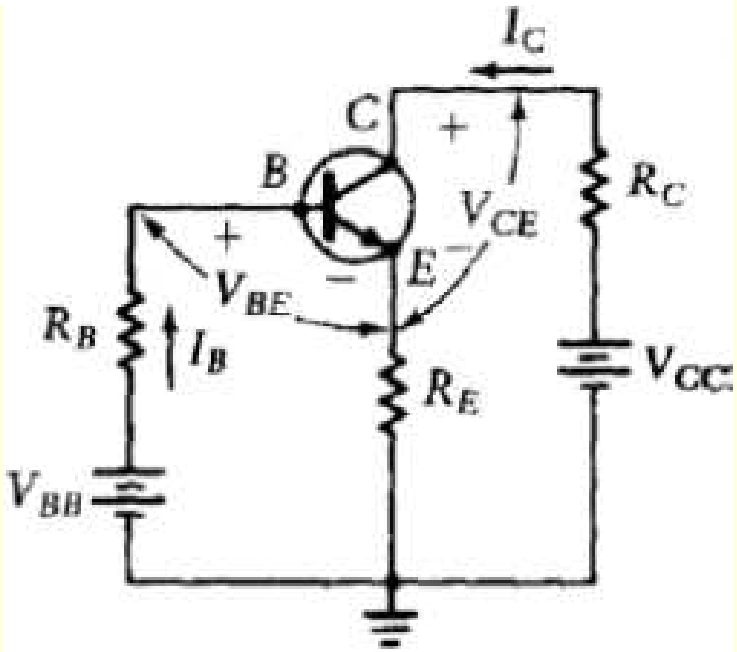
$$I_{CQ} \approx \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E}$$

We can now use equation (2.13) to solve for the quiescent collector current. Letting R_B equal $0.1\ \beta R_E$, we have

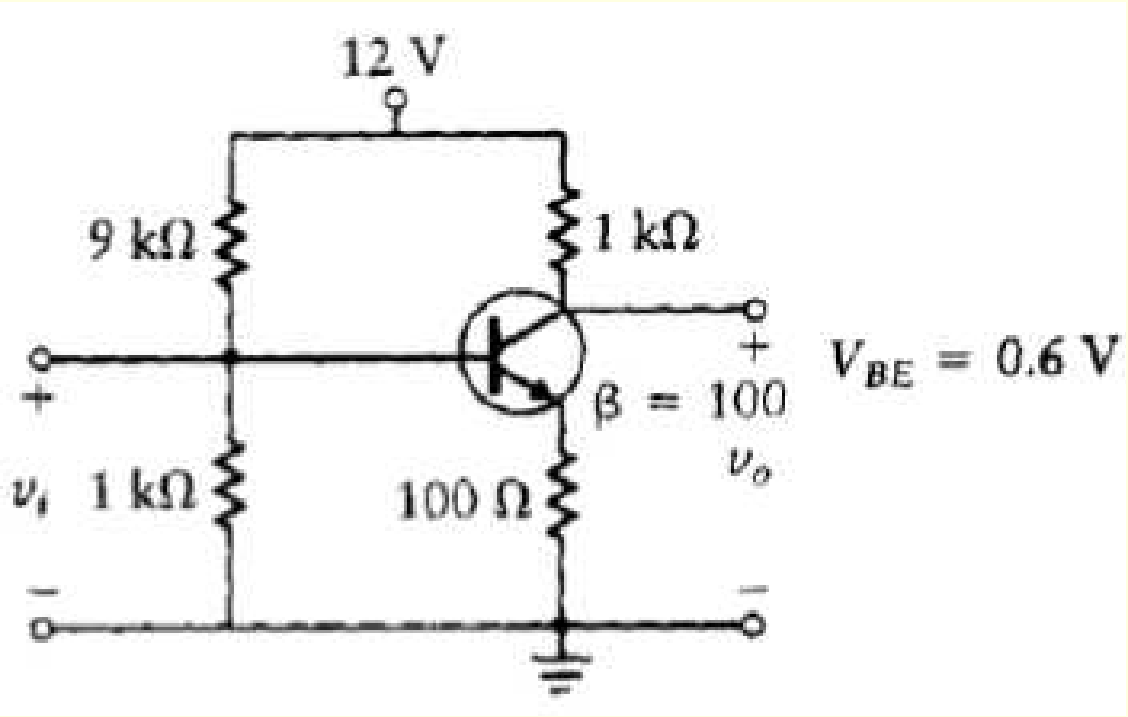
$$I_{CQ} = \frac{V_{BB} - V_{BE}}{0.1\ \beta R_E/\beta + R_E} = \frac{V_{BB} - V_{BE}}{1.1 R_E} \qquad (2.19)$$

Equation (2.19) is used in the design process.



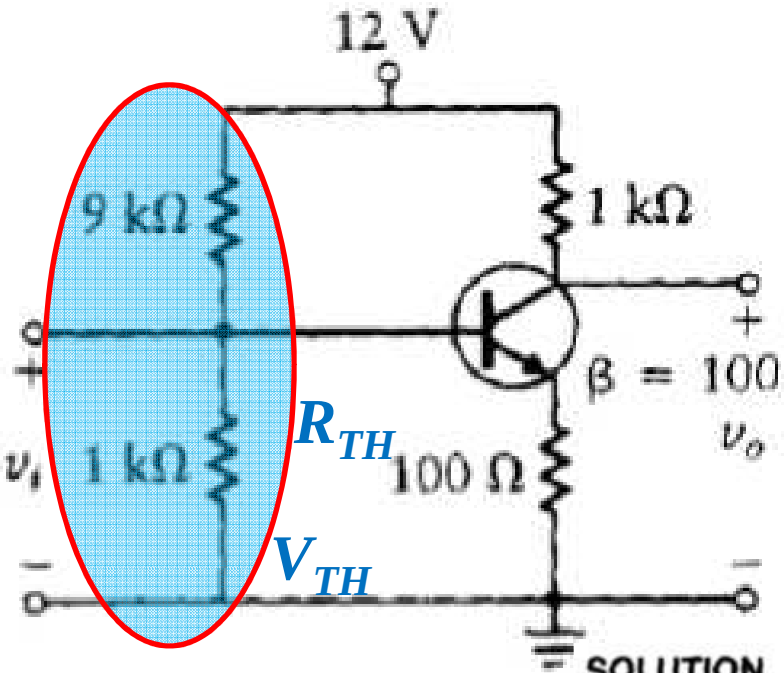


2.5.2 Introduction to Analysis

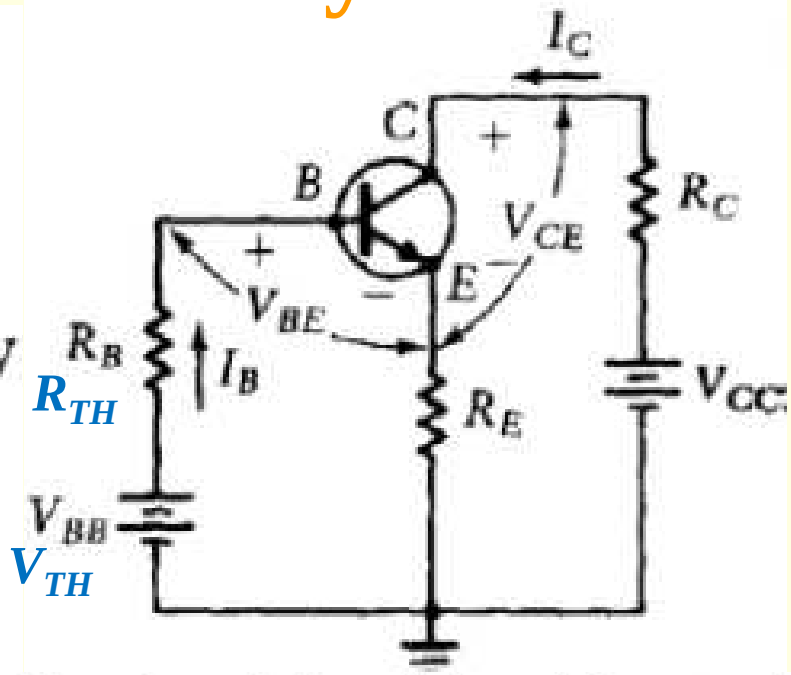


A CE amplifier is configured as shown in Figure 2.17 with $R_1 = 1\ \text{k}\Omega$, $R_2 = 9\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, $V_{CC} = 12\ \text{V}$, $R_E = 100\ \Omega$, $\beta = 100$, and $V_{BE} = 0.6\ \text{V}$. Determine V_{BB}, R_B, and I_{CQ}.

2.5.2 Introduction to Analysis



$V_{BE} = 0.6$ V



SOLUTION We first find the Thevenin equivalent of the resistive network connected to the base.

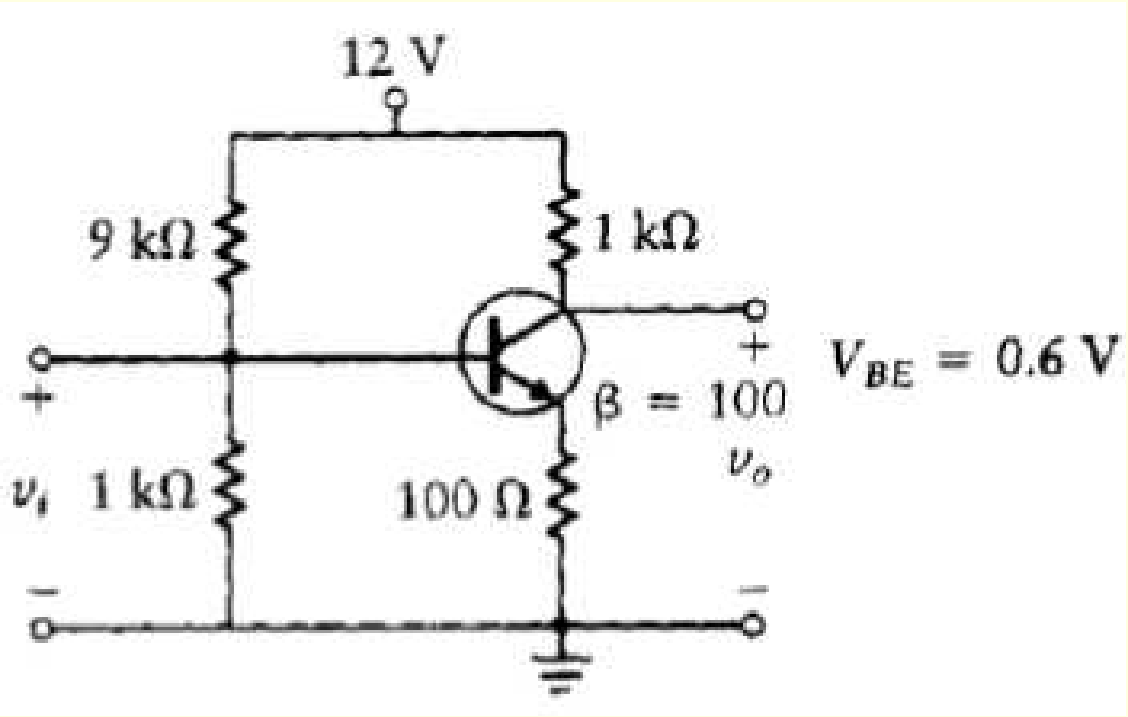
$$V_{BB} = \frac{R_1 V_{CC}}{R_1 + R_2} = \frac{(1000)(12)}{(1000 + 9000)} = 1.2 \text{ V}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = \frac{(1000)(9000)}{(1000 + 9000)} = 900\ \Omega$$

We now use the KVL equation for the base loop, equation (2.13), to obtain

$$I_{CQ} = \frac{V_{BB} - V_{BE}}{R_B/\beta + R_E} = \frac{1.2 - 0.6}{900/100 + 100} = 5.5 \text{ mA}$$

2.5.3 Introduction to Design



In the circuit of Figure 2.17, we wish to place the Q-point in the middle of the load line. Here, $\beta = 100$, $V_{BE} = 0.6$ V, $R_E = 100\ \Omega$, $R_C = 1$ kΩ, and $V_{CC} = 12$ V. Find the required values of R_1 and R_2.

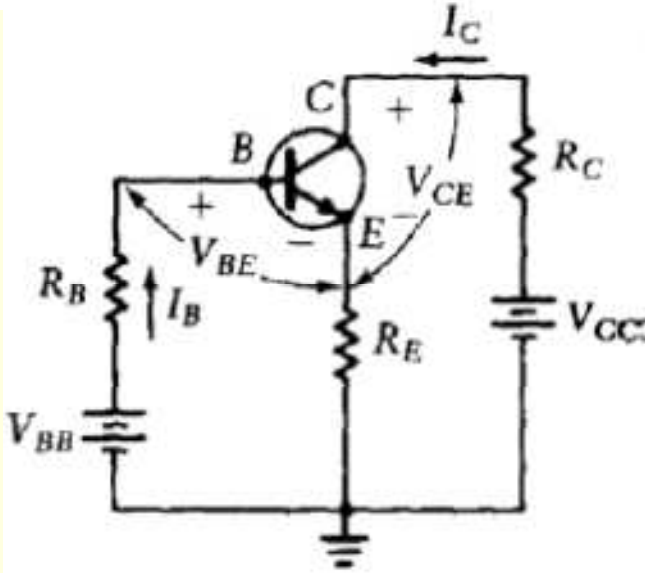
2.5.3 Introduction to Design

SOLUTION The specification that the Q-point is in the middle of the load line requires that

$$V_{CEQ} = \frac{V_{CC}}{2}$$

We can then use KVL around the emitter-collector loop, equation (2.12), to find I_{CQ}:

$$I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_E + R_C} = \frac{V_{CC} - V_{CC}/2}{R_E + R_C} = \frac{12}{2(100 + 1000)} = 5.5 \text{ mA}$$



2.5.3 Introduction to Design

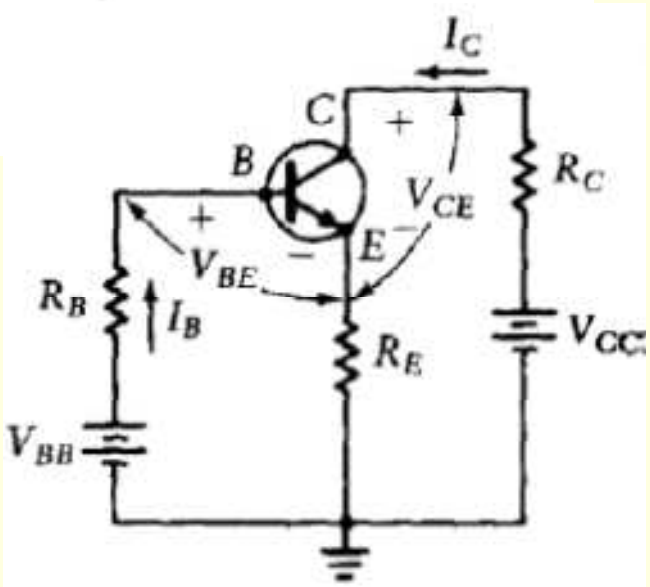
We need to know R_B and V_{BB} in order to find R_1 and R_2. R_B is found from the constraint

$$R_B = 0.1\,\beta R_E = 0.1(100)(100) = 1\,\text{k}\Omega$$

We now use the base loop KVL equation, equation (2.13), to find V_{BB} as follows:

$$V_{BB} = V_{BE} + I_{CQ}\left(\frac{R_B}{\beta} + R_E\right)$$

$$= 0.6 + (0.0055)\left(\frac{1000}{100} + 100\right) = 1.2\,\text{V}$$



2.5.3 Introduction to Design

With V_{BB} and R_B determined, equations (2.16) and (2.17) can be used to find R_1 and R_2.

$$R_2 = \frac{R_B V_{CC}}{V_{BB}} = \frac{1000 \times 12}{1.2} = 10\ \text{k}\Omega$$

$$R_1 = \frac{R_B}{1 - V_{BB}/V_{CC}} = \frac{1000}{1 - 1.2/12} = 1.11\ \text{k}\Omega$$