Prehľad rodín FPGA a CPLD obvodov významných výrobcov

Cieľ prednášky

Predstaviť riešenia FPGA a CPLD obvody najznámejších svetových výrobcov. Prehľad bude zameraný hlavne na najperspektívnejšie rodiny.

Obsah

- Altera,
- Xillinx,
- Actel,
- Lattice

Vývojové kity

- Altera (dostupné na KEMT)

Altera (www.altera.com)

Existujúce rodiny

FPGAs

- Stratix II
- Stratix
- Cyclone II
- Cyclone
- Stratix GX
- APEX II
- APEX 20K
- Mercury
- FLEX 10K
- ACEX 1K
- FLEX 6000

CPLDs

- MAX II
- MAX 3000A
- MAX 7000

Structured ASICs

- About HardCopy
- HardCopy II
- HardCopy Stratix
- HardCopy APEX 20K

Device Family Overview

- CPLDs
- Low-Cost FPGAs
- High-Density FPGAs
- Structured ASICs

Device	General Description	Unique Features
CPLDs MAX II	Lowest-cost, single-chip, easy-to-use CPLD family	• Lowest CPLD cost & power consumption • Highest CPLD density & performance • Instant-on, non-volatile • User flash memory • 1.8-V, 2.5-V & 3.3-V supply voltages
MAX	Low-cost CPLD for lower-complexity, low-density designs	• Low to moderate density • Instant-on, non-volatile • 5-V I/O support • Deterministic timing • 2.5-V, 3.3-V or 5.0-V supply voltages

Low-Cost FPGAs		
Cyclone II	Second-generation, lowest-cost family in the Cyclone™ FPGA series for designs where cost concerns outweigh the need for performance or extensive features	• Nios® II embedded processor support • Embedded 18x18 digital signal processing (DSP) multipliers • Moderate on-chip memory • Moderate-speed I/O & memory interfaces • Broad intellectual property (IP) portfolio support
Cyclone	First-generation, lower-density, low-cost family in the Cyclone FPGA series	• Nios II embedded processor support • Low to moderate on-chip memory • Low to moderate-speed I/O & memory interfaces • Broad IP portfolio support
High-Density FPGAs		
Stratix II	General-purpose FPGA family with the largest density & fastest performance	• Nios II embedded processor support • The most DSP blocks • Large on-chip memory • High-speed I/O & memory interfaces • 1-Gbps dynamic phase alignment (DPA) with source-synchronous signaling • Broad IP portfolio support
Stratix	General-purpose, high-performance FPGA family	• Nios II embedded processor support • DSP blocks • Large on-chip memory • High-speed I/O & memory interfaces • Broad IP portfolio support
Stratix GX	Stratix® architecture with high-speed signaling support	• All Stratix features • 3.125-Gbps transceivers • 1-Gbps DPA • Receiver equalization & transmitter pre-emphasis • Broad IP portfolio

		support
Structured ASICs		
	Low-cost structured ASIC solution with: • Fine-grained structured cell architecture • Prototype with Stratix II FPGA • Same design flow as Stratix II FPGA	• All Stratix II features • Guaranteed seamless migration of FPGA-proven designs • Supported by all major EDA vendors • 50 percent lower power than Stratix II FPGA • 350-MHz performance • Broad IP portfolio support
	Low-cost structured ASIC solution with: • Up to 1 million gates • Prototype with Stratix FPGA • Same design flow as Stratix FPGA	• All Stratix features • Guaranteed seamless migration of FPGA-proven designs • Supported by all major EDA vendors • ~40 percent lower power than Stratix FPGA • ~50 percent higher performance than Stratix FPGA • Broad IP portfolio support

MAX II Device Family Overview

The MAX® II device family is a non-volatile, instant-on programmable logic family with a groundbreaking new CPLD architecture. The new architecture delivers half the cost, one-tenth the power, four times the density, and twice the performance of previous MAX devices. The foundation of these superior results is an architecture that provides all of the advantages of the MAX brand of CPLDs, while leveraging Altera's expertise in look-up table (LUT)-based architectures. The LUT-based architecture delivers the maximum logic capability in the smallest I/O pad-constrained space. As a result, MAX II CPLDs deliver the lowest cost, lowest power, and highest density of any CPLD family.

Based on a cost-optimized 0.18-µm six-layer metal flash process, the MAX II device family has all of the benefits of CPLDs, such as non-volatility, instant-on, ease-of-use, and fast propagation delays. Targeted for general-purpose, low-density logic applications, MAX II devices are ideal for interface bridging, I/O expansion, device configuration, and power-up sequencing. In addition to these traditional CPLD applications, MAX II devices target an extensive number of low-density programmable logic applications previously implemented in FPGAs, ASSPs, and standard logic devices.

MAX II devices offer densities ranging from 240 to 2,210 logic elements (LEs) and up to 272 user I/O pins. Table 1 outlines the MAX II device family members and features. Table 2 shows an overview of MAX II device packaging and I/O pin counts.

Table 1. MAX II Device Overview

Feature	EPM240/G	EPM570/G	EPM1270/G	EPM2210/G
LEs	240	570	1,270	2,210
Typical Equivalent Macrocells	192	440	980	1,700
Maximum User I/O Pins	80	160	212	272
User Flash Memory Bits	8,192	8,192	8,192	8,192
t_{PD1} Corner-to-Corner Performance (ns)	4.7	5.5	6.3	7.1
t_{PD2} Fastest Performance (ns)	3.8	3.7	3.7	3.7
Device Availability	Now	Now	Now	Now

Table 2. MAX II Device Package & Maximum User I/O Pins (1)

Package (Size)	EPM240/G	EPM570/G	EPM1270/G	EPM2210/G
100-Pin Thin-Quad Flat Pack (TQFP) (16 mm x 16 mm)	80	76		
144-Pin TQFP (22 mm x 22 mm)		116	116	
256-Pin FineLine BGA® (2) (17 mm x 17 mm)		160	212	204
324-Pin FineLine BGA (19 mm x 19 mm)				272

Stratix II Device Family Overview

Altera introduces Stratix® II devices, the industry's biggest and fastest FPGAs. Based on the award-winning Stratix device family, Stratix II FPGAs feature a new and innovative logic structure that allows designers to conserve device resources by packing more functionality into less area, dramatically reducing device costs. Built on a 90-nm process technology, the new logic structure delivers on average 50 percent faster core performance and more than twice the logic capacity, and costs 40 percent less than first-generation Stratix devices. Support for internal clock frequency rates of up to 500 MHz and typical design performance at over 250 MHz mean that designers can now get fast system performance with the time-saving advantages inherent in programmable logic solutions.

Based on a 1.2-V, 90-nm, SRAM process, Stratix II devices are available in densities ranging from 15,600 to 179,400 equivalent logic elements (LEs) and up to 9 Mbits of on-chip RAM. Stratix II devices offer up to 384 (18 x18) embedded multipliers in highly optimized digital signal processing (DSP) blocks and source-synchronous differential signaling with dedicated dynamic phase alignment (DPA) circuitry operating at up to 1 Gbps. Stratix II devices also have dedicated serializer/deserializer (SERDES) circuitry to support the LVDS and HyperTransport™ differential I/O electrical standards, and support high-speed communication interfaces—including the 10 Gigabit Ethernet XSBI, SFI-4, SPI-4.2, HyperTransport, RapidIO™, and UTOPIA IV standards. With up to 12 phase-locked loops (PLLs) and 16 global clock networks, the Stratix II FPGA family offers a complete clock management solution including a hierarchical clock structure. In addition, Stratix II devices offer design security, on-chip termination, and remote system upgrade capabilities.

System designers requiring a low-risk cost-reduction path for high-volume production can easily migrate their Stratix II FPGA designs to structured-ASIC production with HardCopy® II devices. HardCopy II devices significantly minimize

migration risk because they are generated directly from a Stratix II FPGA and preserve the Stratix II architecture's high density, high performance, industry-leading functionality, and enhanced timing features. This seamless migration process guarantees first-time success for high-volume production, rewarding system designers with minimum time-to-market at the lowest cost.

Table 1 outlines the Stratix II device family members and features. Table 2 shows an overview of Stratix II device packaging and I/O pin counts.

Table 1. Stratix II Device Overview

Feature	Device					
	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
Adaptive Logic Modules (ALMs) *(1)*	6,240	13,552	24,176	36,384	53,016	71,760
Equivalent Logic Elements (LEs) *(1)*	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM Blocks (512 Bits + Parity)	104	202	329	488	699	930
M4K RAM Blocks (4 Kbits + Parity)	78	144	255	408	609	768
M-RAM Blocks (512 Kbits + Parity)	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,448	6,747,840	9,383,040
DSP Blocks	12	16	36	48	63	96
Embedded Multipliers *(2)*	48	64	144	192	252	384
PLLs *(3)*	6	6	12	12	12	12
Maximum User I/O Pins	366	500	718	902	1,126	1,170
Availability	Now	Now	Now	Now	Now	Now

Notes to Table 1:

1. Each ALM is equivalent to 2.5 logic elements (LEs).
2. Each DSP block in Stratix II devices can implement four 18×18 multipliers or one 36×36 multiplier. To obtain the total number of 36×36 multipliers per device, divide the total number of 18×18 multipliers by a factor of 4.
3. Includes both fast and enhanced PLLs.

Table 2. Stratix II Device Package & Maximum User I/O Pins

Package Size (mm x mm)	Device					
	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
484-Pin FineLine BGA® (FBGA) Package (23 x 23)	342	342	334			
484-Pin Hybrid FBGA (27 x 27)				308 *(1)*		
672-Pin FBGA (27 x 27)	366	500	492			
780-Pin FBGA (29 x 29)				534 *(1)*	534 *(1)*	
1,020-Pin FBGA (33 x 33)			718	758	742	742
1,508-Pin FBGA (40 x 40)				902	1,126	1,170

Cyclone II FPGA Family Overview

Altera® Cyclone™ II devices are designed on an all-layer-copper, low-k, 1.2-V SRAM process and are optimized for the smallest possible die size. Built on TSMC's highly successful 90-nm process technology using 300-mm wafers, Cyclone II devices offer higher densities, more features, exceptional performance, and the benefits of programmable logic at ASIC prices. Cyclone II devices offer from 4,608 to 68,416 logic elements (LEs) and are designed with an optimal set of features, including embedded 18 x 18 multipliers, dedicated external memory interface circuitry, 4-kbit embedded memory blocks, phase-locked loops (PLLs), and high-speed differential I/O capabilities.

Cyclone II devices extend the reach of FPGAs further into cost-sensitive, high-volume applications, continuing the success of the first-generation Cyclone device family. Table 1 outlines the Cyclone II FPGA family's features and availability.

Table 1. Cyclone II FPGA Overview

Device	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM Blocks (4 kbits + 512 Parity Bits)	26	36	52	105	129	250
Total RAM Bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded 18 x 18 Multipliers	13	18	26	35	86	150
PLLs	2	2	4	4	4	4
Maximum User I/O Pins	142	182	315	475	450	622
Differential Channels	58	77	132	205	193	262
Availability (1)	Q3 2005	Q3 2005	Q2 2005	Now	Q3 2005	Q2 2005

***Note to Table 1**:*

1. More information on the lead times for these devices is available from local Altera sales representatives.

Table 2 shows an overview of Cyclone II device packaging and user I/O pin counts.

Table 2. Cyclone II Device Packages & Maximum User I/O Pins

Package Size (mm x mm)	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
144-Pin TQFP (1) **(22 x 22)**	89	85				
208-Pin PQFP (2) **(30.35 x 30.35)**	142	138	(4)			
256-Pin FineLine BGA (3) **(17 x 17)**	(4)	182	152			
484-Pin FineLine BGA (23 x 23)			315	322	294	
672-Pin FineLine BGA (27 x 27)				475	450	422
896-Pin FineLine BGA (31 x 31)						622

Notes to Table 2:

1. TQFP = Thin quad flat pack
2. PQFP = Plastic quad flat pack
3. BGA = Ball-grid array
4. These devices will be supported in a future version of the Quartus® II software. Contact Your local Altera sales representative for more information.

Table 3 shows the appropriate configuration devices to use for Cyclone II devices.

Table 3. Appropriate Configuration Devices for Cyclone II FPGAs

Configuration Device	Cyclone II Devices Supported					
	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
EPCS1	X					
EPCS4	X	X	X			
EPCS16	X	X	X	X	X	X
EPCS64	X	X	X	X	X	X

MAX 3000A CPLD Family Overview

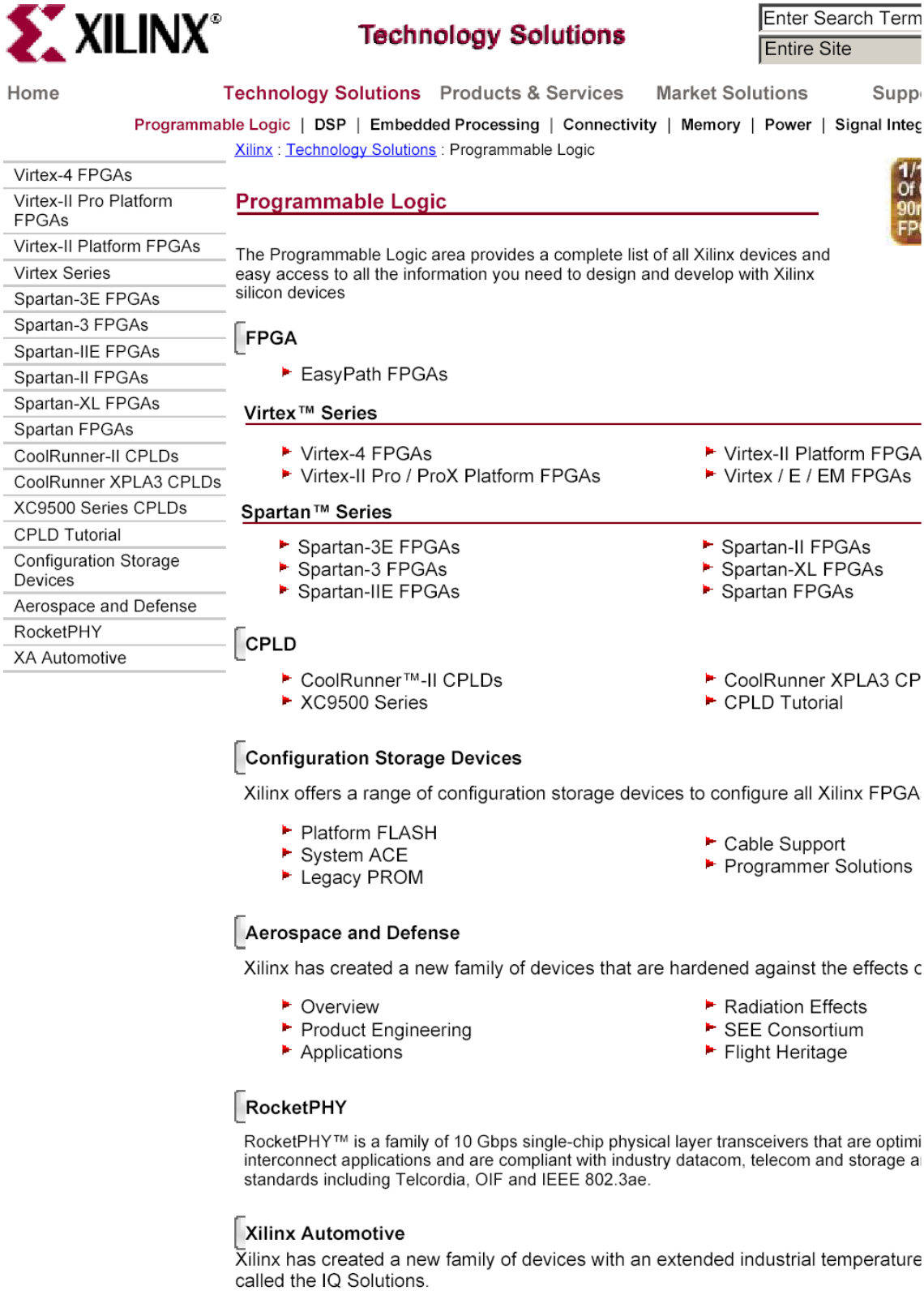
Altera's MAX® 3000A CPLD family is manufactured on a cost-optimized 0.30-µm, four-layer-metal process, and ranges in density from 32 to 512 macrocells. Available in both commercial and industrial grades in popular speed grades and packages, the 3.3-V MAX 3000A CPLD family is ideal for cost-sensitive, high-volume applications.

Table 1 lists the MAX 3000A device offerings.

Table 1. MAX 3000A Device Overview (3.3 V)

Feature	Device				
	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A
Usable Gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Maximum User I/O Pins	34	66	96	158	208
t_{PD} (ns) *(1)*	4.5	4.5	5.0	7.5	7.5
t_{SU} (ns) *(2)*	2.9	2.8	3.3	5.2	5.6
t_{CO1} (ns) *(3)*	3.0	3.1	3.4	4.8	4.7
f_{CNT} (MHz) *(4)*	227.3	222.2	192.3	126.6	116.3
Package	**I/O Pins**				
44-Pin PLCC *(5)*	34	34			
44-Pin TQFP *(6)*	34	34			
100-Pin TQFP		66	80		
144-Pin TQFP			96	116	
208-Pin PQFP *(7)*				158	172
256-Pin FineLine BGA® *(8)*			98	161	208

Xilinx (www.xilinx.com)



Virtex-4 FPGA Family Capabilities

Virtex-4™ family FPGAs offer the functionality and performance to address the widest range of demanding applications. We began with the industry-leading capabilities of Virtex-II Pro devices. Then we added enhancements that accelerate productivity by simplifying system design and providing the margin that makes it easy to achieve design targets.

Virtex-4 Capabilities simplify system design

- **Most Flexible High Peformance Logic Architecture: CLB**
  - Compact utilization for reduced device cost
  - Up to 200,000 logic cells-the industry's highest density ever

- **Advanced, System Clock Management: Xesium™ clocking technology**
  - Achieve highest system performance
  - Abundance of fully flexible clocking resources
  - Minimized clock jitter and skew
  - New clock generation features and control

- **Complete Memory Resources: Smart RAM Memory Hierarchy**
  - Build the right memory for any application
  - Small, local memories: distributed RAM (up to 1.36 Mb) and SRL16
  - Medium, integrated: block RAM (up to 10 Mbit); configure multi-rate FIFOs without consuming logic resources
  - Large, external: create interfaces to the latest high-speed memory devices, including DDR2/DDR SDRAM, QDR II SRAM, RLDRAM II, and FCRAM II

- **Ultimate Parallel Connectivity: SelectIO™**
  - 1+ Gbps differential I/O
  - 600 Mbps single-ended I/O
  - ChipSync source-synchronous technology
  - Eliminate external resistors with built-in XCITE DCI active I/O termination — series, parallel, differential
  - 16 I/O banks for flexible implementation of various interfaces simultaneously within th esame device

- **Comprehensive Serial Connectivity: RocketIO™**
  - Implement industry-standard and custom serial protocols to connect or bridge "anything to anything" with RocketIO serial transceivers
  - Up to 24 transceivers, each providing 622 Mbps to 11.1 Gbps, full duplex operation

- **Ultra-high-performance DSP: XtremeDSP Slice**

- Configure XtremeDSP slice to over 40 DSP and arithmetic functions
- Up to 256 GMACS (18x18) performance using 512 XtremeDSP slices

Embedded Processing: PowerPC™ Processor

- Up to two 450MHz, 700+ DMIPS embedded IBM PowerPC 405 Processor hard cores
- Auauxiliary Processor Unit (APU) controller simplifies the integration of hardware accelerators and coprocessors
- Implement the industry's fastest soft processing solution with our MicroBlaze™ core

Ethernet Connectivity: Tri-Mode Ethernet MAC

- Integrated Ethernet media access controller (MAC)
- 10/100/1000 Mbps performance
- UNH-verified compliance

Enhanced Design Security: Secure Chip AES

- Protect your design with maximum security IP protection
- Embedded 256-bit AES Encryption
- Part of standard configuration flow

Xilinx Virtex-4 Series FPGAs

		Virtex-4 LX (Logic)								Virtex-4 SX (Signal Processing)			Virtex-4 FX (Embedded Processing & Serial Connectivity)					
		XC4VLX15	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	XC4VFX12	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140
CLB Resources	CLB Array (Row x Column)	64 x 24	96 x 28	128 x 36	128 x 52	160 x 56	192 x 64	192 x 88	192 x 116	64 x 40	96 x 40	128 x 48	64 x 24	64 x 36	96 x 52	128 x 52	160 x 68	192 x 84
	Slices	6,144	10,752	18,432	26,624	35,840	49,152	67,584	89,088	10,240	15,360	24,576	5,472	8,544	18,624	25,280	42,176	63,168
	Logic Cells	13,824	24,192	41,472	59,904	80,640	110,592	152,064	200,448	23,040	34,560	55,296	12,312	19,224	41,904	56,880	94,896	142,128
	CLB Flip Flops	12,288	21,504	36,864	53,248	71,680	98,304	135,168	178,176	20,480	30,720	49,152	10,944	17,088	37,248	50,560	84,352	126,336
Memory Resources	Max. Distributed RAM Bits	98,304	172,032	294,912	425,984	573,440	786,432	1,081,344	1,425,408	163,840	245,760	393,216	87,552	136,704	297,984	404,480	674,816	1,010,688
	Block RAM/FIFO w/ECC (18 kbits each)	48	72	96	160	200	240	288	336	128	192	320	36	68	144	232	376	552
	Total Block RAM (Mbits)	864	1,296	1,728	2,880	3,600	4,320	5,184	6,048	2,304	3,456	5,760	648	1,224	2,592	4,176	6,768	9,936
Clock Resources	Digital Clock Managers (DCM)	4	8	8	8	12	12	12	12	4	8	8	4	4	8	12	12	20
	Phase-matched Clock Dividers (PMCD)	0	4	4	4	8	8	8	8	0	4	4	0	0	4	8	8	8
I/O Resources	Max Select I/O™	320	448	640	640	768	960	960	960	320	448	640	320	320	448	576	768	896
	Total I/O Banks	9	11	13	13	15	17	17	17	9	11	13	9	9	11	13	15	17
	Digitally Controlled Impedence	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Max Differential I/O Pairs	160	224	320	320	384	480	480	480	160	224	320	160	160	224	288	384	448
	I/O Standards	LDT-25, LVDS-25, LVDSEXT-25, BLVDS-25, ULVDS-25, LVPECL-25, LVCMOS25, LVCMOS18, LVCMOS15, PCI33, LVTTL, LVCMOS33, PCI-X, PCI66, GTL, GTL+, HSTL I (1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2I, SSTL2II, SSTL18 I, SSTL18 II																
DSP Resources	XtremeDSP™ Slices	32	48	64	64	80	96	96	96	128	192	512	32	32	48	128	160	192
Embedded Hard IP Resources	PowerPC™ Processor Blocks	—	—	—	—	—	—	—	—	—	—	—	1	1	2	2	2	2
	10/100/1000 Ethernet MAC Blocks	—	—	—	—	—	—	—	—	—	—	—	2	2	4	4	4	4
	RocketIO™ Serial Transceivers	—	—	—	—	—	—	—	—	—	—	—	0	8	12	16	20	24
Speed Grades	Commercial (slowest to fastest)	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11, -12	-10, -11
	Industrial (slowest to fastest)	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10, -11	-10
	Configuration Memory Bits	4,765,568	7,819,904	12,259,712	17,717,632	23,291,008	30,711,680	40,347,008	51,367,808	9,147,648	13,700,288	22,745,216	4,765,568	7,242,624	13,550,720	21,002,880	33,065,408	47,856,896
	EasyPath™ Cost Reduction Solutions[1]	—	XC4VLX25	XC4VLX40	XC4VLX60	XC4VLX80	XC4VLX100	XC4VLX160	XC4VLX200	XC4VSX25	XC4VSX35	XC4VSX55	—	XC4VFX20	XC4VFX40	XC4VFX60	XC4VFX100	XC4VFX140

Spartan-IIE Product Overview

You are facing tremendous design challenges. Rapidly evolving standards, shifting market requirements, intense competition, and the demands for lower costs make your job more difficult than ever before. How do you create new consumer products on schedule and under budget, without losing your peace of mind?

To be successful in this tough, competitive marketplace, you need a fast, inexpensive, and flexible design solution that you can re-program in the lab and at your customer's site. You need fast, reliable performance, and the lowest cost per I/O pin in the industry - that's what you get with Spartan□IIE FPGAs. There is no faster, safer, or lower cost way to develop next-generation consumer products.

The Lowest Cost Solution for Consumer Applications

Spartan-IIE FPGAs give you everything you need to create cost-optimized, flexible, feature-rich products; and you'll find they're far easier (and less expensive) to develop than any ASIC. With the Spartan-IIE family, you get:

- Densities from 50K to 600K system gates
- Superior I/O capabilities
    - Up to 514 I/O - more than any other low-cost FPGA
    - Supports 19 standards, including LVDS, HSTL, and PCI
- A low cost per I/O of any programmable solution
- A seamless path for density migration
- A robust feature set - You get DLLs, distributed RAM, and block RAM, delivering the resources you need to develop today's digital convergence products.
- The MicroBlaze soft processor - Reduce your overall design cost and device count with this low cost, easy-to-use soft processor solution (an excellent field programmable controller).
- XtremeDSP - You get over one billion MACs/sec/dollar, the most cost-effective programmable DSP solution.
- ISE software tools - You'll finish your design faster, and reduce your development costs even further.
- Extensive IP core support - We offer a wide range of cores including PCI and DSP algorithms, to increase your productivity and decrease design time.

Spartan-IIE Family at a Glance

Feature/ Product	XC2S50E	XC2S100E	XC2S150E	XC2S200E	XC2S300E	XC2S400E	XC2S600E
System Gates	50K	100K	150K	200K	300K	400K	600K
Logic Cells	1,728	2,700	3,888	5,292	6,912	10,800	15,552
BRAM (Kbits)	32	40	48	56	64	160	288
Delay Lock Loops (DLL)	4	4	4	4	4	4	4
Max. Dist.	24	37.5	54	73.5	96	150	216
RAM (Kbits)							
Max Available User I/O	182	202	265	289	329	410	514
Package	**User I/O**	**User I/O**	**User I/O**	**User I/O**	**User I/O**	**User I/O**	**User I/O**
PQ208	146	146	146	146	146		
TQ144	102	102					
FT256	182	182	182	182	182	182	
FG456		202	265	289	329	329	329
FG676						410	514

CoolRunner-II Product Overview

Get the benefits of CoolRunner-II RealDigital CPLDs for your next design:

- As low as 28.8µW standby power
- Up to 323MHz performance
- Unparalleled design security
- Highest I/O count per macrocell

CoolRunner-II Features and Benefits

Features	Benefits
32 to 512 macrocell device selection	Wide range of densities for multiple applications
1.8 volt supply voltage with 1.5 to 3.3V I/Os	Eliminates the need for voltage converters
Four levels of design security	Prevents pattern theft
RealDigital CPLD technology	Advanced low power, high speed programmable logic
DataGATE	Unique features for power saving
Multiple I/O banking	Supports different voltage levels in the same device
Input hysteresis and programmable grounds	Improved signal integrity for high speed I/O
Dual edge-triggered flip-flops/ ClockDivide	Higher performance and more versatility compared to any competing solution
Multiple LVCMOS, HSTL, SSTL I/O	Flexible I/O supporting wide range of device interface
Advanced packaging	Low cost small form factor micro lead frame packages
Superior pin locking	Easy redesign during development and enables field upgradability

CoolRunner-II Product Overview

Feature/Product	XC2C 32A	XC2C 64A	XC2C 128	XC2C 256	XC2C 384	XC2C 512
Macrocells	32	64	128	256	384	512
T_{pd}(ns)	3.8	4.6	5.7	5.7	7.1	7.1
f_{SYS} (MHz)	323	263	244	256	217	179
I/O Banks	2	2	2	2	4	4
Packages	**User I/O**	**User I/O**	**User I/O**	**User I/O**	**User I/O**	**User I/O**
QF32	21					
VQ44	33	33				
PC44	33	33				
QF48		37				
CP56	33	45				
VQ100		64	80	80		
CP132			100	106		
TQ144			100	118	118	
PQ208				173	173	173
FT256				184	212	212
FG324					240	270

Xilinx Automotive (XA)

The Xilinx Automotive (XA) product family is the industry's leading programmable logic family developed specifically for automotive applications. This family is ideal for a wide range of advanced automotive electronics modules and systems ranging from the latest Driver Assistance Systems and Infotainment systems to Reconfigurable Instrument Clusters and ECU Gateways. These applications benefit from the flexibility, reconfigurability and advanced on-chip resources such as multipliers for high speed DSP provided in devices from the Xilinx automotive industries leading PLD supplier. XA devices include:

- Extended temperature ranges, both Automotive Industrial and Automotive Q-Grade
- Full PPAP support
- Industry-recognized AEC-Q100 device-qualification flow

Xilinx is committed to quality and offers a roadmap to address the worldwide automotive quality standard ISO TS 16949, as well as Pb-free packaging to meet the RoHS directive.

	Temperature / Grade	
Product Group	**Automotive I**	**Automotive Q**
XA FPGA	T_J = -40°C to +100°C	T_J = -40°C to +125°C
XA CPLD	T_A = -40°C to 85°C	T_A = -40°C to +125°C

Device Family				
FPGA	**CPLD**	**Packages**	**Densities**	**Special Feature**
Spartan-3		VQG100, PQG208, FTG256, FTG465	50k - 1000k System Gates	Embedded Multipliers for DSP & Digital Clock Management to solves high speed design challenges
Spartan-IIE		TQ144 & FT256	50k - 300k Systems Gates	Embedded DLLs for clock management, Embedded Memory and 19 I/O Standards
	CoolRunner-II	VQG44 & VQG100	32 - 256 Macrocells	Ultra Low Power & up to 8 single ended I/O standards
	9500XL	VQ44 & TQ144	36 - 144 Macrocells	Lowest cost per macrocell
Platform Flash Configuration Memory		VO20	1 - 4 Mb	In-system programmable

Actel (www.actel.com)

Flash Devices

- ProASIC3: Flash based, reprogrammable devices 30k to 3 million gates
- ProASIC PLUS: Flash based, reprogrammable devices 75k to 1 million gates
- ProASIC: Flash based, reprogrammable devices 100k to 450k gates

Antifuse Devices

- Axcelerator: High-speed antifuse FPGAs with gate densities of up to 2 million equivalent gates
- SX-A / SX: Antifuse devices 8k to 72k gates
- eX: Antifuse devices 3k to 12k gates
- MX: Antifuse devices 3k to 54k gates

ProASIC3

High Performance, Low Cost FLASH FPGAs the only true ASIC alternative

The ProASIC3/E families of Flash FPGAs offer a breakthrough in price, performance, density, and features for today's most demanding applications. The ProASIC3/E families are based on nonvolatile Flash technology and support between 30k to 3M gates and up to 616 high performance I/Os.

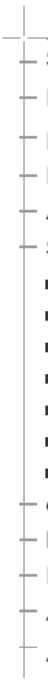
Product Table

	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000	A3PE600	A3PE1500
System Gates	30 k	60 k	125 k	250 k	400 k	600 k	1 M	600 k	1.5 M
VersaTiles (D-Flip-Flop)	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	38,400
RAM kbits (1,024 bits)	-	18	36	36	54	108	144	108	270
4,608-Bit Blocks	-	4	8	8	12	24	32	24	60
FlashROM (FROM) bits	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLLs	-	1	1	1	1	1	1	6	6
VersaNet Globals	6	18	18	18	18	18	18	18	18
I/O Standards	Std. & Hot Swap	Std.+	Std.+	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Std.+/ LVDS	Pro	Pro
I/O Banks (+JTAG)	2	2	2	4	4	4	4	8	8
Single-Ended I/O / Differential I/O Pairs*									
QN132	81								
VQ100	79	71	71	68/13					
FG144		96	97	97/24	97/24	97/24	97/24		
TQ144		91	100						
PQ208			133	151/34	151/33	154/35	154/35	147/65	147/65
FG256				157/38	178/38	179/45	179/45	165/79	
FG484					194/38	227/56	288/68	270/135	280/136
FG676									439/209
FG896									

Flash Benefits

Features:	Benefits:
Low Cost	The world's lowest cost FPGA solution offering industry-leading unit cost and lo system cost.
High Performance	Enhanced, high-performance architecture up to 350MHz operation and 95% logi utilization.
Single Chip	Does not require additional configuration nonvolatile memory in order to load th configuration data at every system power-up, which reduces cost and increases and system reliability.
Live-At-Power-Up	Greatly simplifies system design, making the device available to perform critica setup tasks and reduce bill-of-materials costs and PCB area.
Secure ISP	Support of built-in AES decryption engine and industry-leading Flash-based AE for secure remote field updates over public networks with encrypted bitstream.
User Nonvolatile Memory	1,024 bits of on-chip, user accessible, nonvolatile FlashROM (FROM) that can b diverse system applications.
Low Power	Maximizes power savings with very limited power-on current surge and no high- transition period, both of which occur on many FPGAs. Offers low dynamic pow consumption.
Firm Errors Immune	Flash cell configuration element cannot be altered by high-energy neutrons and therefore immune, unlike SRAM based FPGAs.
Device Security	Utilizes a 128-bit Flash-based lock and inherent Flash technology features, pro most impenetrable security for programmable logic designs.

SX-A / SX FPGAs: Reducing the Cost of Performance



Actel's SX-A/SX devices can match the speed and performance of an ASIC or be used to generate system wide savings by integrating multiple functions into a low-cost single-chip solution. Providing a combination of high speed and low-power SX-A/SX decreases the premium for performance while providing a solution highly secure from reverse engineering.

The low cost of integration:
Today's applications require higher speeds and greater density than ever before. Actel's SX-A/SX FPGA families open the door to next generation designs that could not previously be implemented in programmable logic. The expanded capabilities and performance allow products to get to market faster, cost less and generate more revenue.

The industries highest design security:
The interconnections within SX-A FPGAs are extremely small, are densely distributed throughout the device, and do not leave an observable signature that can be electrically probed or visually inspected. With these safeguards, SX-A devices are virtually immune to copying and reverse engineering.

SX-A / SX Benefits:

- 12,000 to 108,000 usable system gates
- 3.7ns clock-to-output (pin-to-pin)
- 350MHz internal clock frequency
- 66MHz, 64-bit 3.3V/5.0V PCI performance (supporting Target, Master and Master/Target)
- Hot swappable I/Os (SX-A)
- Excellent for ATM, IP, WDM, DBE and SONET applications
- Able to run at OC3 to OC192 data rates
- 2.5V, 3.3V, and 5.0V mixed voltage support
- 100% resource utilization with 100% pin locking
- Low power consumption (less than 1W @ 200MHz)
- Complete BST/JTAG support

A54SX-A / SX Selector Guide

	SX08/08A	SX16/16A	SX16P	SX32/32A	SX72A
Typical Gates	8,000	16,000	16,000	32,000	72,000
System Gates	12,000	24,000	24,000	48,000	108,000
Dedicated Flip Flops	256	528	528	1080	2012
Maximum I/O	130	177	177	249	360
Logic Modules	768	1452	1452	2880	6036

Lattice (www.latticesemi.com)

Leadership FPGA Devices From Lattice

Overview

FPGA (Field Programmable Gate Array) solutions from Lattice bring together innovative FPGA architecture and advanced technology in unique ways to deliver performance and cost goals for a wide variety of applications.

Learn about the Lattice FPGA technology roadmap.

High-Volume FPGAs

- LatticeECP-DSP (EConomyPlus-DSP) FPGA devices combine the optimized LatticeEC fabric with a high-performance embedded sysDSP block that is tailored for the implementation of common DSP functions. See the LatticeECP FPGA Selector Table below.

- LatticeEC (EConomy) FPGA devices deliver an optimized blend of features, cost and performance for high-volume, cost sensitive applications. See the LatticeEC FPGA Selector Table below.

Non-Volatile Infinitely Reconfigurable FPGAs

- **ispXP™** Technology brings together "Instant-On" and High Security and other attributes of non-volatile technologies with the re-configurability of SRAM in a single device. By providing internal non-volatile cells for storing FPGA configuration, customers simplify their designs; they do not require external Boot Prom and thus save space and cost. A non-volatile array distributed within the FPGA device stores the device configuration. At power-up the configuration is transferred from FLASH memory to configuration SRAM in less than 1mS. By eliminating the external configuration bit stream and by providing a security scheme that prevents program read-back, these devices deliver secure FPGA solutions.

- The **LatticeXP™** (eXpanded Programmability) FPGA family combines the optimized FPGA architecture used in the LatticeEC (EConomy) family with ispXP technology implemented on a low-cost 130nm FLASH process to provide "Instant-On", High Security, Non-Volatile, and Reconfigurable features - in a single low-cost chip. See the LatticeXP FPGA Selector Table below.

LatticeECP and EC Product Family Selector Guide

Device	sysDSP Blocks*	18 x 18 Embedded Multipliers*	LUTs (K)	Distributed RAM (K)	EBR Block SRAM (K)	Number of EBR SRAM Blocks	MAX User I/O	PLLs
EC1	-	-	1.5	6	18	2	112	2
EC3	-	-	3.1	12	55	6	160	2
ECP6/EC6	4	16	6.1	25	92	10	224	2
ECP10/EC10	5	20	10.2	41	277	30	288	4
ECP15/EC15	6	24	15.4	61	350	38	352	4
ECP20/EC20	7	28	19.7	79	424	46	400	4
ECP33/EC33	8	32	32.8	131	535	58	496	4

* ECP Devices only

LatticeXP FPGA Product Family Selector Guide

Device	LUTs (K)	Distributed RAM (K)	EBR Block SRAM (K)	Number of EBR SRAM Blocks	Max User I/O	PLLs
LFXP3						
3.1	12	54	6	136	2	
LFXP6						
5.8	23	90	10	188	2	
LFXP10						
9.7	39	216	24	244	4	
LFXP15						
15.4	61	288	32	300	4	
LFXP20						
19.7	79	414	46	340	4	

ispXPGA Product Family Selector Guide

Family	FPGA System Gates (K)	sysHSI Channels*	LUTs (K)	Logic FFs (K)	Block RAM (K)	Distributed RAM (K)	Max User I/O
ispXPGA 125/E	139	4	1.9	3.8	92	30	176
ispXPGA 200/E	210	8	2.7	5.4	111	43	208
ispXPGA 500/E	476	12	7.1	14.1	184	112	336
ispXPGA 1200/E	1,250	20	15.4	30.8	414	246	496

Note: 8 PLLs with global clocks and low-skew clock nets per device.
* "E-Series" does not support sysHSI.

Altera Development Kits

Altera® development kits provide a complete, high-quality design environment for engineers. A wide variety of kits help simplify the design process and reduce time-to-market. Development kits include software, reference designs, cables, and programming hardware. Table 1 lists Altera development kits.

Table 1. Altera Development Kits (1)

Product Name	Device	Price
High-Speed Development Kit, Stratix GX Edition	Stratix GX EP1SGX40	$7,995
DSP Development Kit, Stratix Professional Edition	Stratix EP1S80	$4,995
PCI High-Speed Development Kit, Stratix Professional Edition	Stratix EP1S60	$4,995
Nios II Development Kit, Stratix Professional Edition Updated	Stratix EP1S40	$2,495
DSP Development Kit, Stratix Edition	Stratix EP1S25	$1,995
DSP Development Kit, Stratix II Edition NEW	Stratix II EP2S60	$1,995
High-Speed Development Kit, Stratix II Edition NEW	Stratix II EP2S60	$1,995
PCI Development Kit, Stratix Edition	Stratix EP1S25	$1,995
DSP Development Kit, Cyclone II Edition NEW	Cyclone II EP2C35	$995
Nios II Development Kit, Cyclone Edition Updated	Cyclone EP1C20	$995
Nios II Development Kit, Cyclone II Edition NEW	Cyclone II EP2C35	$995
Nios II Development Kit, Stratix Edition Updated	Stratix EP1S10	$995
Nios II Development Kit, Stratix II Edition NEW	Stratix II EP2S30	$995
PCI Development Kit, Cyclone II Edition NEW	Cyclone II EP2C35	$995
Nios II Evaluation Kit NEW	Cyclone EP1C12	$295
MAX II Development Kit NEW	MAX II EPM1270	$150

University Program Education Kits

The Altera® University Program offers participating universities a UP3 Education Kit with the complete Quartus® II design software. This kit (shown in Table 1) provides a comprehensive solution to the programmable logic design challenge.

Table 1. University Program Education Kits

UP3 Education Kit

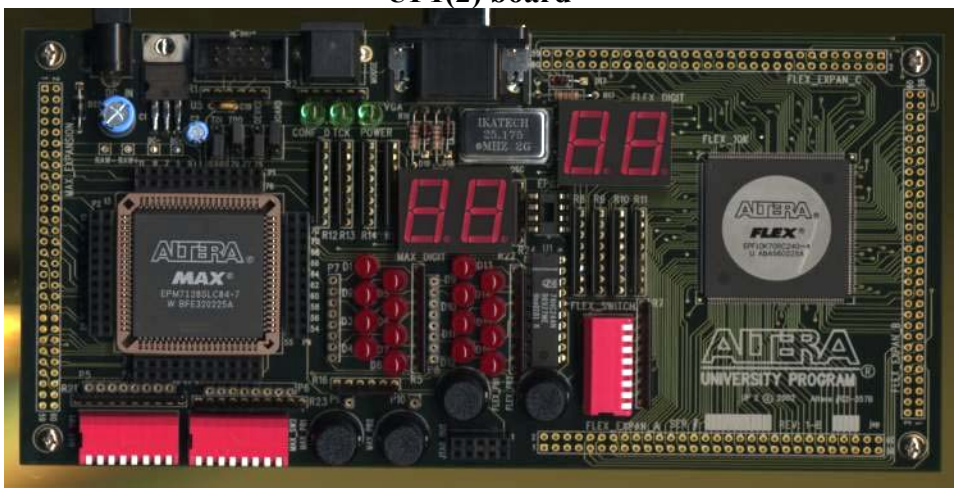
- Quartus II development software, version 4.1
- UP3 development board with a Cyclone™ EP1C6Q240C8 device
- ByteBlaster™ II download cable
- Power supply
- Kit price: $249 USD

UP2 Education Kit

- Quartus II development software, version 4.0
- UP2 development board with a FLEX 10K® EPF10K70 device
- ByteBlaster download cable
- Power supply
- Digital Design and Implementation with Field Programmable Devices by Zainalabedin Navabi
- Kit Price: $149 USD

Note: Altera strongly recommends using the UP3 education kit over the UP2 kit due to the versatile rich features embedded in it. The UP3 kit comes with the industry's most advanced logic development software tool along with other leading edge products.

UP1(2) board



UP3 board – www.slscorp.com

Similar to UP3 hardware

Embedded System Development Kit

The Embedded System Development Kit provides a powerful, low-cost solution for prototyping and rapid development of the products. The ESDK in conjunction with 8051 IDE is an excellent means for system designing, prototyping, emulation and simulation.

The ESDK board comes with a powerful Altera Cyclone FPGA. It gives scope to a hardware design engineer to design, prototype and test IP cores or any hardware design using HDLs like Verilog or VHDL. Using 8051 IDE, one can simulate and test “C” or assembly code. The entire environment helps to quickly implement any processor as well as any real time operating system on the ESDK. The IP for an 8051 micro controller is pre-built and may be loaded into the FPGA. Using the 8051 IDE, programs may be downloaded and executed on the system. The ESDK board has industry standard interconnections, memory subsystem, multiple clocks for system design, JTAG configuration and expansion headers for greater flexibility and additional user interfaces.

The 8051 board can be used for DSP applications by interfacing directly to a DSP processor or implementing DSP functions inside the FPGA. In short, it is a dual-purpose kit, which can be used for prototyping and developing VLSI designs as well as designing and developing microprocessor based embedded systems.

The ESDK is shipped with Altera Quartus II software starter CD and download cable. Henceforth, cost of buying expensive FPGA design software is saved.

Fetures

- Powerful Development Board for FPGA designs
  - Provides an Altera EP1C6Q240 Device and EPCS1 Configuration device
  - Supports intellectual property based (IP-based) design both with and without a microprocessor.
- Industry standard interconnection

    - USB 2.0 compliant (full & low speed)
    - Two RS 232 Ports
    - Parallel Port (IEEE1284)
    - PS/2 Port
- Memory Sub System
    - 1Mbyte of SRAM
    - 2Mbytes of FLASH
    - 2Kbytes of I2C PROM (expandable)
- Multiple Clocks for system design
- JTAG Configuration and debugging
- Expansion headers for greater flexibility and capacity
    - 5V Santa Cruz long Expansion Card Header provides 72 I/O for the development of additional boards providing various functionality
- Additional user interface features
    - One user-definable 4-bit switch block
    - Four user-definable push button switches and one global reset switch
    - Four user-definable LEDs
    - One 16x2 character display LCD Module
    - I2C Real Time Clock
- 8051 IDE

Applications

ESDK board is a general-purpose board with lot many peripheral supports.

- With FPGA on the board, the user can develop/test any program written in Hardware Description Language.
- All the peripherals on the board are connected to the I/O lines of the FPGA, so the user can download and test any application related to the available peripherals on the board.
- The ESDK board provides one parallel port and two serial ports to develop/test the applications.
- Applications based on USB, PS2, and I2C etc can be developed/tested.
- The ESDK board is having a 16X2 character LCD which serves as a display device.
- 1Mbyte of SRAM, 2Mbytes of FLASH and 2Kbytes of I2C PROM are provided to develop/test memory related applications.
- ESDK board is shipped with the pre-built 8051 IP core to develop micro controller related applications.
- 8051 IDE includes Cross Compiler, Assembler, Simulator and Emulator.
    - **Cross Compiler and Assembler:** Supports Assembly, C and mixed language ('C' + Assembly) programming and creates ROMable code / Intel HEX format file
    - **Simulator:**SLS 8051 IDE Simulator provides all the necessary features to simulate user code.
    - **Emulator:**SLS 8051 IDE Emulator provides all the necessary features for emulation. Some of them are listed below:
        - Read and modify internal registers (registers and SFRs)
        - Read and modify external RAM locations
        - Run from a memory location
        - Load an Intel Hex file from the host computer in RAM
        - Single-step execution of a program
        - Call a user program as a subroutine
        - Dump memory data to a terminal
        - Set upto 4 breakpoints

DSP Development Kit, Stratix II Edition

The DSP Development Kit, Stratix® II Edition delivers a complete digital signal processing (DSP) development environment for design engineers. The kit facilitates the entire design process from design conception through hardware implementation. The DSP Development Kit, Stratix II Edition includes the Stratix II DSP development board, DSP Builder development tool, Quartus® II development software, MATLAB/Simulink evaluation software, evaluation intellectual property (IP) cores, system reference designs and labs, as well as power supplies, cables, and documentation.

Development Kit Contents

The DSP Development Kit, Stratix II Edition features:

- DSP development board, Stratix II edition
  - Stratix II EP2S60F1020C4 device
- Analog I/O
  - Two-channel, 12-bit, 125-million samples per second (MSPS) analog-to-digital (A/D)
  - Two-channel, 14-bit, 165-MSPS digital-to-analog (D/A)
  - VGA digital-to-analog converter (DAC)
  - Stereo audio coder/decoder (CODEC), 96 KHz
- Digital I/O
  - Connector for Texas Instruments' (TI's) C6000 DSP Starter Kit (DSKs) to enable peripheral expansion and FPGA co-processing
  - Two 40-pin connectors for Analog Devices' A/D converter evaluation boards
  - Mictor connector for Agilent and Tektronix logic analyzers
  - RS 232 serial port
  - 10/100 Ethernet physical layer/media access control (PHY/MAC) and RJ-45 jack
- Memory
  - 32-Mbyte SDR SDRAM
  - 16-Mbyte flash
  - 1-Mbyte SRAM
  - 16-Mbyte compact flash
- MATLAB/Simulink evaluation software
- DSP Builder development tool
- Quartus II DKE
- Evaluation IP cores
- System reference designs & labs
  - DSP Builder Filtering Design
  - DSP Builder/SOPC Builder Image Processing Reference Design
  - Fast Fourier Transform (FFT) Co-Processor Reference Design for TI's TMS320C6416 DSK
  - Nios® II reference designs
- Cables & accessories
  - USB-Blaster download cable
  - Serial cable (RS-232)
  - Power supply
  - International power cords

DSP Development Kit, Stratix Edition

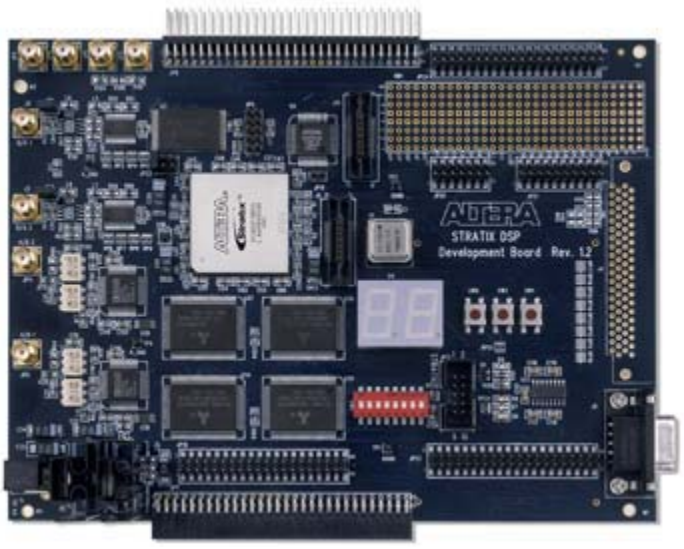
The DSP Development Kit, Stratix® Edition contains everything you need to create your digital signal processing (DSP) design from start to implementation in hardware. The items included in the kit provide you with a complete out-of-the-box experience. In addition to power supplies, cables, and documentation, the kit includes the Stratix DSP development board, DSP Builder, Quartus® II development software, MATLAB/Simulink evaluation software, evaluation intellectual property (IP) cores, and system reference designs/labs.

Development Kit Contents

The DSP Development Kit, Stratix Edition includes the following:

- EP1S25 Stratix device
- Quartus II design software
- DSP development board, Stratix edition
  - Stratix EP1S25F780 device
  - Analog I/O pins
    - 2-channel, 12-bit, 125 million samples per second (MSPS) analog-to-digital (A/D)
    - 2-channel, 14-bit, 165 MSPS digital-to-analog (D/A)
- Cables and accessories
  - ByteBlaster™ II parallel download cable
  - Serial cable (RS-232)
  - Power supply
  - International power cords
- Many hardware and software reference designs targeted to the DSP Development Board, Stratix Edition
- Coupon for a 20 percent discount on any one instructor-led Altera® Technical Training course scheduled in North America

Figure 1. DSP Development Kit, Stratix Edition



Nios II Development Kit, Cyclone Edition

Altera's Nios® II Development Kit, Cyclone™ Edition provides everything needed for system-on-a-programmable-chip (SOPC) development. Based on Altera's Nios II family of embedded processors and the low-cost Cyclone EP1C20 device, this development kit provides an ideal environment for developing and prototyping a wide range of price-sensitive embedded applications.

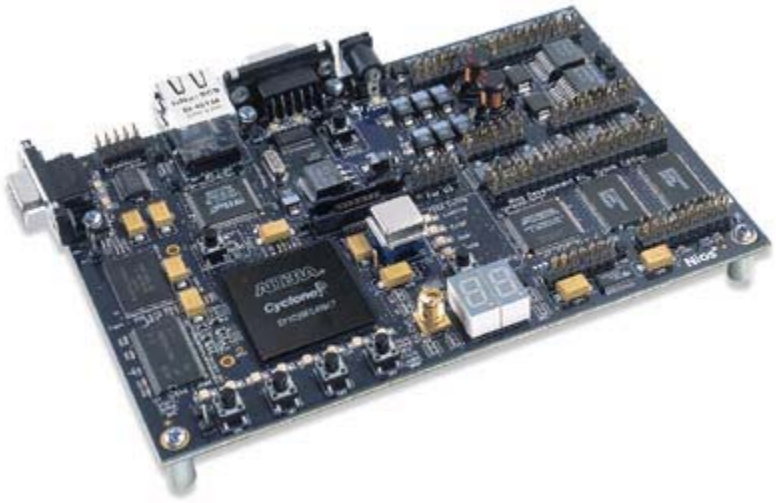
The Nios II Development Kit, Cyclone Edition contains everything needed for system-level design, whether the user has a background in hardware, software, or both hardware and software.

Development Kit Contents

The Nios II Development Kit, Cyclone Edition includes the following:

- Nios II family of embedded processors, soft embedded core configurable processor
- Nios II integrated development environment (IDE)
- µC/OS-II real-time operating system port & TCP/IP stack
- Nios II instruction set simulator (ISS)
- Library of standard microprocessor peripherals
- Quartus® II design software, including the SOPC Builder system development tool
    - One-year license
    - Windows platform only
- Nios development board, Cyclone edition (shown in Figure 1)
    - Cyclone EP1C20FC400 device
    - MAX® EPM7128AE CPLD configuration control logic
    - SRAM (1 Mbyte in two banks of 512 Kbytes, 16-bit wide)
    - SDR SDRAM (16 Mbytes, 32-bit wide)
    - Flash (8 Mbytes)
    - EPCS4 Serial Configuration Device (4 Mbits)
    - CompactFlash connector header for Type I CompactFlash cards (40 available user I/O pins)
    - 10/100 Ethernet physical layer/media access control (PHY/MAC)
    - Ethernet connector (RJ-45)
    - Two serial connectors (RS-232 DB9 port)
    - Two 5-V-tolerant expansion/prototype headers (2 x 41 available user I/O pins)
    - Two Joint Test Action Group (JTAG) connectors
    - Mictor connector for debugging
    - Four user-defined push-button switches
    - Eight user-defined LEDs
    - Dual 7-segment LED display
    - Power-on reset circuitry
- Cables & accessories
    - USB Blaster download cable
    - Parallel extension cable (6 feet)
    - Serial cable (RS-232)
    - 9-V power supply
    - International power cords
    - LCD module
    - CompactFlash card (16 Mbytes)
    - Ethernet (RJ45) cable (7 feet)
    - Ethernet crossover adapter
- Many hardware and software reference designs targeted to the Nios development board, Cyclone edition
- One-year subscription to Nios II processor-related tool upgrades (This subscription does not include Quartus II software updates. The Altera® Software Subscription includes the Quartus II design software. There are no license or royalty fees connected with the Nios II development kit used to develop with Altera FPGAs and HardCopy™ devices.)
- Coupon for a 20% discount on any one instructor-led Altera Technical Training course scheduled in North America

Figure 1. Nios Development Board, Cyclone Edition



Software Development Tools

Software engineers do not need any prior FPGA design experience to use the Nios II Development Kit, Cyclone Edition. Altera's Nios II IDE provides a complete embedded software design environment for the Nios II family of embedded processors, with facilities for:

- C/C++ code entry & editing
- Project management & compilation
- Software debugging
- Flash programming

This kit includes world-class development tools and complete documentation as well as multiple reference designs and a step-by-step software development tutorial (available in the on-line help browser) to get users up and running immediately. Users can write, compile, and run software on their Nios development boards within minutes of opening the box.

The Nios II instruction set simulator (ISS) allows users to begin developing programs before the target hardware platform is ready. The Nios II IDE lets users run programs on the ISS as easily as running them on a real hardware target.

Altera provides ports of the µC/OS-II real-time operating system and the Lightweight IP TCP/IP stack. The µC/OS-II RTOS is built on the thread-safe HAL system library, and implements a simple, well-documented RTOS scheduler. The TCP/IP stack is built on µC/OS-II, and implements the standard UNIX Sockets API.

Documented software example designs are provided to demonstrate all prominent features of the Nios II processors and the development environment.